A REVIEW OF LOW VOLTAGE AND LOW POWER CMOS ADDERS USING VLSI DESIGN IN VERILOG/VHDL

Lokesh S
Department of Electrical and Electronics Engineering
University College of Engineering, BIT campus,
Anna University, Trichy, Tamil Nadu, India.

Abstract - The dominant portion of power dissipation in CMOS adder circuits, due to logic transitions, varies as the square of the supply, significant savings in power dissipation may be exacted by operating with reduced supply voltage. If the supply voltage is reduced while threshold voltage stays same, the noise margins will reduce. Addition is a crucial process because it usually involve carry ripple steps which must propagate a carry signal from each bit to it’s higher bit position. This results in a substantial circuit delay. The adder which lies in the crucial delay path will effectively determine the system overall speed. To improve noise margins, the threshold voltages must also be made smaller. However sub-threshold leakage current increases exponentially when threshold voltage is reduced. The higher static dissipation may then offset the reduction in transitions portion of the dissipation. Hence, a formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell, that is fully compensated for threshold voltage drop in MOS transistors presented. This new cell can reliably operate within certain bounds when the power voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. Low Power design is required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

II. 4 BIT PARALLEL ADDER

A single full adder performs the addition of two one bit numbers and an input carry. But a Parallel Adder is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. It consists of 4 full adders connected in a chain where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain. Parallel adders normally incorporate carry look ahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed.

I. INTRODUCTION

Low Power Design of VLSI circuits have been identified as critical technological need in recent years due to high demand for portable consumer electronic products. In this regard many innovative designs for basic logic functions using pass transistors and transmission gates have appeared in literature recently. These designs relied on the intuition and cleverness of the designers, without involving formal design procedures. Hence, a formal design procedure for realizing a minimal transistor CMOS pass network XOR-XNOR cell, that is fully compensated for threshold voltage drop in MOS transistors presented. This new cell can reliably operate within certain bounds when the power voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. Low Power design is required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

II. 4 BIT PARALLEL ADDER

A single full adder performs the addition of two one bit numbers and an input carry. But a Parallel Adder is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. It consists of 4 full adders connected in a chain where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain. Parallel adders normally incorporate carry look ahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed.

Fig.1 Logic Diagram of 4 Bit Parallel Adder

A) Boolean Equation of 4 Bit Parallel Adder:
For the SUM (S) bit:
SUM = (A XOR B) XOR Cin = (A ⊕ B ⊕ Cin)
For the CARRY-OUT (Cout) bit:
CARRY-OUT = (A AND B) OR (B AND Cin) OR (Cin AND A).

B) Truth Table of 4 Bit Parallel Adder

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Cin</th>
<th>Sum</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

C) Gate level Design of 4 Bit Parallel Adder

III. 4 BIT RIPPLE CARRY ADDER (RCA)
The basic unit of Ripple Carry Adder is a full adder. It can be extended indefinitely to any number by connecting the carry-out of the previous 1-bit Full Adder to the carry-in of the next 1-bit Full Adder. Of all the adder architectures RCA offers good performance, nonetheless, its delay characteristics depend heavily on the length of the carry propagation path, thus making it a relatively unfavorable choice for circuits with nonrandom input operands. The worst-case delay increases linearly with the length of the carry propagation path, which depends on number of bits processed by operands, n. Also the area of the adder is proportional to n. Therefore in situations when high speed performance is crucial and the minimum amount of hardware is underperforming, using a RCA in an arithmetic operation would be detrimental. One of the most serious drawbacks of this adder is that each full adder has to wait for the carry out of the previous stage to output steady state result. Therefore even if the adder has a value at its output terminal, it has to wait for the carry before the output reaches a correct value. Generally speaking the worst-case delay of RCA is when a carry signal transition ripples through all stages of adder chain from the least significant bit to the most significant bit, which is approximated by,

\[ t = (n-1)(tc + ts) \]

\( tc = \text{Delay through the carry stage} \)
\( ts = \text{Delay through the sum stage} \)
\( n = \text{no of bits of full adder} \)

D) Output of 4 Bit parallel Adder

E) 4 Bit Parallel Adder’s Propagation Delay time simulated from synthesis report with XPower Simulation
IV. 4 Bit Carry Look Ahead Adder (CLA)

It is an adder with time propagation duration in \(O(\log n)\) and whose area size requirement is in \(O(n \log n)\). The delay time of CLA architecture therefore exhibits logarithmic dependency on the size of the adder, which allows the propagation delay of the carry signal to be minimized.
Fig. 3 Logic Diagram of 4 Bit Carry Look Ahead Adder

Ci has to overcome 2 gates (AND & OR) in order to produce Ci+1.

**Carry Propagate = 2n**

n - number of bits.

For 4 bit adder n = 4; therefore Carry Propagate = 8

It has to overcome 8 gate levels to produce resultant carry.

The Propagate P and generate G in a full-adder, is given as:

\[ P_i = A_i \oplus B_i \] (Carry propagate)

\[ G_i = A_i \cdot B_i \] (Carry generate)

The new expressions for the output sum and the carryout are given by:

\[ S_i = P_i \oplus C_i \]

\[ C_{i+1} = G_i + P_i \cdot C_i \]

These equations show that a carry signal will be generated in two cases:

1) if both bits \( A_i \) and \( B_i \) are 1

2) if either \( A_i \) or \( B_i \) is 1 and the carry-in \( C_i \) is 1.

The general expression is

\[ C_{i+1} = G_i + P_i \cdot G_i - 1 + P_i - 1 \cdot G_i - 2 + \ldots + P_i - 1 \cdot P_0 \cdot C_0. \]

A) Boolean Equation of 4 Bit Carry Look Ahead Adder

\[ P_i = A_i \oplus B_i \] Carry propagate

\[ G_i = A_i \cdot B_i \] Carry generate

\[ S_i = P_i \oplus C_i \]

\[ C_{i+1} = G_i \oplus P_i \cdot C_i \]

C0 - (1) to be given as an input

\[ C_1 = G_0 \cdot P_0 \cdot C_0 - (2) \]

\[ C_2 = G_1 + P_1 \cdot G_0 + P_1 \cdot C_0 - (3) \]

\[ C_3 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot C_0 - (4) \]

\[ C_4 = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0 - (5) \]

B) Truth Table of 4 Bit Carry Look Ahead Adder

C) Gate Level Design of 4 Bit Carry Look Ahead Adder

D) Output of 4 Bit Carry Look Ahead Adder

E) 4 Bit Carry Look Ahead Adder Delay time simulated from synthesis report with XPower Simulation
V. 4 Bit Carry Select Adder (CSL)

It is a particular way to implement an adder that computes (n+1) bit as a sum of two (n) bit numbers. CSL adder is simple but faster than other adders. In CSL both the n-bit operands $A_i$ and $B_i$ are divided into k blocks of possibly different sizes. The additional cost of the CSL over the RCA is the duplicate carry chain and the select logic. Then CSL adder using a multiplexer, depending on the real carryout, the correct sum is chosen. The delay of n-bit carry select adder based on an m-bit CLA blocks can be given by the following equation when using constant carry number blocks, 

$$T = t_{seup} + m \times t_{carry} + \left(\frac{n}{m}\right) \times t_{mux} + t_{sum}$$

And by the following equation when using successively incremented carry number blocks respectively,

$$T = t_{seup} + m \times t_{carry} + \left(2n\right)^{0.5} \times t_{mux} + t_{sum}.$$ 

---

A) Truth Table of 4 Bit Carry Select Adder

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

---

B) Gate Level Design of 4 Bit Carry Select Adder

![Gate Level Design of 4 Bit Carry Select Adder](image)

---

C) Output of 4 Bit Carry Select Adder

![Output of 4 Bit Carry Select Adder](image)

---

D) 4 Bit Carry Select Adder Propagation Delay time simulated from synthesis report with XPower Simulation

![4 Bit Carry Select Adder Propagation Delay](image)
VI. 4 BIT CARRY SAVE ADDER (CSA)

A CSA tree consists of CSA operators and one adder at the root of the tree. The CSA operators are used to transform an arbitrary number of operands in the addition process to produce two adding operands, after which the adder at the root of the CSA tree computes final sum. Unlike RCA, CLA, CSL adders, the CSA realizes the concurrent addition of multiple operands, which is a basic requirement of multiplication. Instead of using the 2-operand adders that necessitate the time consuming carry propagation to repeat several times, depending on the number of operands, the CSA’s timing could be improved with a little increase or even a reduction in area. Time to obtain Summation is given by,

\[ T = (k-2) \text{ AND } T_{csa} \text{ OR } T_{cpa}. \]

Fig.5 Logic Diagram of 4 Bit Carry Save Adder

A) Boolean Equation of 4 Bit Carry Save Adder

\[
\text{SUM} = (A \text{ XOR } B) \text{ XOR } C_{in} = (A \oplus B \oplus C_{in})
\]

\[
\text{CARRY-OUT} = (A \text{ AND } B) \text{ OR } (B \text{ AND } C_{in}) \text{ OR } (C_{in} \text{ AND } A).
\]

B) Gate Level Design of 4 Bit Carry Save Adder

C) Output of 4 Bit Carry Save Adder

D) 4 Bit Carry Save Adder Propagation Delay time simulated from synthesis report with XPower Simulation
VII. 4 BIT CARRY SKIP ADDER (CSK)

A CSK adder is similar to how the MCC adder works, which is to reduce the carry propagation time by skipping over groups of successive adder stages. In general, with the assumption that the delay of the skip logic is equal to the carry propagation delay from one stage to another, the overall time of the carry propagation chain is calculated as follows,

$$T_{\text{carry}} = (K-1) + (n/K - 2) + (K-1) \text{ stages.}$$

K refers to an n-bit CSK with fixed block size.

The design of Carry Skip Adder that achieves low power dissipation and high performance operation. The CSK adder’s delay and power dissipation are reduced by dividing the adder into variable-sized blocks that balance the delay of inputs to carry the chain. This grouping active power by minimizing extraneous glitches and transitions.

A) Boolean Equation of 4 Bit Carry Skip Adder

$$P_i = A_i \oplus B_i$$

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = (A_i \land B_i) \lor (P_i \land C_i)$$

B) Gate Level Design of 4 Bit Carry Skip Adder

C) Output of 4 Bit Carry Skip Adder

D) 4 Bit Carry Skip Adder Propagation Delay time simulated from synthesis report with XPower Simulation
VIII. 4 Bit Conditional Sum Adder (COS)

The underlying principle of this architecture is the parallel computation of two sets of conditional sums and conditional carries for each bit position. To minimize the computation time, the given ‘n’ bits are divided into smaller groups so that the serial carry propagation within the groups can be carried out in parallel. The COS approach is very similar to CSL. The major difference is that in COS the division of the n bits into sub-blocks continues until the extreme of having only single-bit adders if n is an integer power of 2. The COS scheme can still be implemented even if n is not a power of 2 because sub-blocks of equal sizes are not compulsory.

A) Boolean Equation of 4 Bit Conditional Sum Adder

\[ S_i^0 = A_i \oplus B_i \]
\[ C_{i+1}^0 = A_i \cdot B_i \]
\[ S_i^1 = A_i \oplus B_i \]
\[ C_{i+1}^1 = A_i + B_i \]

B) Gate Level Design of 4 Bit Conditional Sum Adder

C) Output of 4 Bit Conditional Sum Adder

D) 4 Bit Conditional Sum Adder Propagation Delay time simulated from synthesis report with XPower Simulation

Fig. 7 Logic Diagram of 4 Bit Conditional Sum Adder
IX. PERFORMANCE EVALUATION OF CMOS ADDERS

An overall performance evaluation and comparison, to rank the adders has been carried out based on 1.2 micro-meter CMOS technology.

<table>
<thead>
<tr>
<th>LOGIC STYLE</th>
<th>INPUT BIT</th>
<th>AVERAGE INPUT VOLTAGE (V)</th>
<th>AVERAGE INPUT POWER (W)</th>
<th>PROPAGATION DELAY (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.082</td>
<td>1.551</td>
</tr>
<tr>
<td>Ripple Carry Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.082</td>
<td>1.65</td>
</tr>
<tr>
<td>Carry Look-ahead Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.081</td>
<td>1.545</td>
</tr>
<tr>
<td>Carry Select Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.086</td>
<td>1.948</td>
</tr>
<tr>
<td>Carry Save Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.082</td>
<td>2.350</td>
</tr>
<tr>
<td>Carry Skip Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.082</td>
<td>2.094</td>
</tr>
<tr>
<td>Conditional Sum Adder</td>
<td>4 Bit</td>
<td>1.7</td>
<td>0.080</td>
<td>0.279</td>
</tr>
</tbody>
</table>

Fig.8 Performance Comparison of Different Logic Style CMOS Adders.

X. CONCLUSION

CMOS Adders [Parallel Adder, RCA Adder, CLA Adder, CSL Adder, CSA Adder, CSK Adder, COS Adder] has been analyzed which exhibits a higher speed and lower power consumption compared with those of the conventional one. Delay, Power and area are the constituent factors in VLSI design that limits the performance of any circuit. The proposed design of all the CMOS Adders were simulated and synthesized in Xilinx ISE 14.7 and the source code is written in Verilog / VHDL, and the Power analysis is simulated in X Power Analysis. Since the conditional sum adder deals with carry generation and sum generation separately, and the carry propagation is performed faster than the sum propagation, its operation speed can be improved with a propagation delay of 0.279 ns with a power consumption of 0.080 watts. The speed enhancement was achieved by modifying the structure through the complementary transmission gate logic. The static and dynamic power dissipation in CMOS Adders were minimized by VLSI design. The Propagation Delay has been reduced and thus Performance characteristics for these adders are tabulated.

XI. REFERENCE


