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THE EFFECT OF CHANNEL AND GATE LENGTH OF LDMOS DEVICE ON ITS PERFORMANCE

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Abstract - **In this paper, the DC and AC characteristics of LDMOS transistor has been investigated. The parameters of LDMOS device namely breakdown voltage (BV), on-resistance, transconductance output conductance, cut off frequency and maximum frequency of oscillation have been studied with varying channel and gate length. A compact model of lateral double diffused MOS (LDMOS) transistor having small size with different characteristics have been presented in this paper. This investigation revealed some improved in on-resistance and breakdown voltage, cut off frequency (f_T) and maximum frequency of oscillation (f_{max}) of this device. All characteristics have been simulated by a two dimensional device simulator.**

Keywords— **LDMOS, Breakdown Voltage, Cut off Frequency, Gain, On-Resistance.**

I. INTRODUCTION

The growth in personal communications systems, TV broadcast and cellular base stations is rapidly accelerating worldwide. There are a number of different modulation and access schemes including GSM, CDMA and WLL. The emergence of new communication standards has put a key challenge for semiconductor industry to develop RF devices that can handle high power and high frequency simultaneously. Over the past decades, semiconductor device researchers have proposed many challenging devices and technologies for growing of high power, high frequency, high temperature, high linearity and high efficiency communication system. Si transistors, hetero-structure bipolar transistors (HBTs), SiGe HBTs, GaAs high electron mobility transistors (HEMTs) and SiC metal semiconductor field effect transistors (MESFETs) have achieved a standard position in these areas and RF devices play a key role in the design of power amplifiers (PAs), which is considered as a heart of base station. LDMOS devices have been dominating in the communication field since last decade and are still widely used for PA design and development. LDMOS is the one of these devices used for high power and high frequency applications. This paper deals with the optimization of RF-LDMOS transistor [1]-[4].

Initially the RF-LDMOS is studied in TCAD for the improvement in RF performance. The physical intrinsic structure of RF-LDMOS is provided by Infineon Technologies AG. A reduced surface field (RESURF) of low doped drain (LDD) region is considered in detail because it plays an important role in RF-LDMOS devices to obtain high breakdown voltage (BV). But on the other hand, it also reduces the RF performance due to high on- resistance (Ron). The excess interface state charges at the RESURF region are introduced to reduce the Ron, which not only increases the dc drain current, but also improve the RF performance in terms of power, gain and efficiency. The important achievement is the enhancement in operating frequency up to 4 GHz. In LDD region, the effect of excess interface charges at the RESURF is also compared with dual implanted-layer of p type and n-type. The comparison revealed that the former provides 43 % reduction in Ron with BV of 70 V, while the later provides 26 % reduction in Ron together with BV of 64 - 68 V. Therefore, the motivation of this brief is to explore structure modification in LDMOS to enhance its high voltage and high frequency capabilities [5]-[20].

This paper compare the transconductance, output conductance, cut off frequency **(f_t)** and maximum frequency of oscillation **(f_{max})** with variation of gate length and channel length.

II. LDMOS FEATURES/STRUCTRURES

A transformed low power LDMOS transistor presents several features which improved their RF properties from a low power MOSFET [21]. The fig.1 and fig.2 show the general and simulated structure of a LDMOS transistor. In this fig, the drift region consists of a low doped n well diffusion in a p type substrate and channel region is formed by lateral diffusion of a p base implantation. The poly-silicon gate length is 0.75 um and channel length is 0.3 um. Due to low doped of n well, depletion region are enhanced in LDMOS transistor so that BV and Ron are higher and RF performance are degraded.

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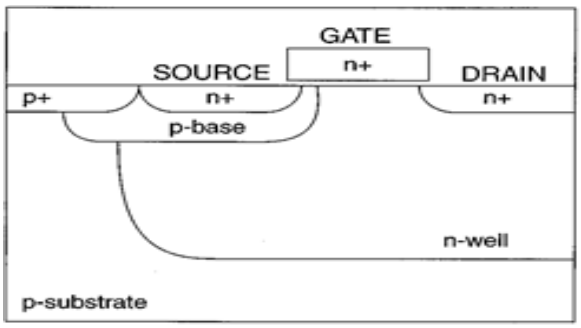

Fig.1. Schematic/reference diagram of LDMOS.

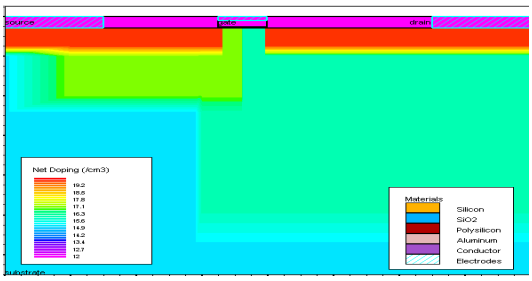

Fig. 2. Simulator based LDMOS model.

A. **Modelling of LDMOS using device Simulation-**

A device structure for simulation was created using process simulation that includes the actual process details used for fabrication. Two dimensional numerical simulations of the device have been used for simulation. The models viz. drift-diffusion equations, Poisson and SRH (Shockley-Read-Hall) are considered for generation-recombination; FLDMOB and CVT model for velocity saturation-mobility; and IMPACT SELB for impact ionization. These simulations methods allow taking into account carrier–carrier scattering in the high doping concentration, carrier velocity saturation, dependence of mobility on temperature and vertical electric influence. Breakdown mechanism is also investigated by both two dimensional process simulations using IMPACT SELB model. The device simulation was then used to reproduce the measurement DC and AC characteristics. Using 2D device simulations, LDMOS is shown to exhibit significant improvement in BV, R_{on}, g_m, f_t and f_{max}.

III. RESULTS & DISCUSSIONS

Many analytical models and some first order equations are used for optimization of DC and AC characteristics of device.

B. **DC characteristics**

DC analysis provides the current voltage characteristics, threshold voltage, breakdown voltage (BV), on-resistance (Ron), and transconductance (g_m). DC analysis is taken by current-voltage (IV) characteristics; input gate voltage and output drain current as shown in Fig.3 in which drain current is plotted against drain voltage from 0V to 6 V with gate biasing between 1V to 10V. For lower Vgs value, the difference between two curves is not very distinct, but for greater Vgs values, the drain current for LDMOS is lower due to the Ron.
Drain current flows only if gate voltage exceeds the threshold voltage following the relation.

$$Id = Idss(Vgs - Vth)^2 \qquad (1)$$

And threshold voltages for LDMOS device are shown in fig.4, in which threshold voltage decreases with increase the drain voltage whereas V_{ds} has value 0.1V, 1V and 2V and threshold voltage reach 1.7V, 1.6V and 1.4V respectively.
Hence the theoretical and simulation studies show that LDMOS has lower drain current flow than compare to conventional NMOS because LDMOS has higher on resistance (R_{on}) which produced due to addition of n well region [22]. The theoretical investigations conclude that the R_{on} and BV of LDMOS device depends on lightly doped drain region (LDD). The on resistance and BV increases with decrease doping in drift/n well region. Basically the R_{on} consists of the channel resistance, the drift region resistance and substrate resistance. Hence in this simulation, we simulate the R_{on} with influence of gate and channel length, keeping LDD region length small and other

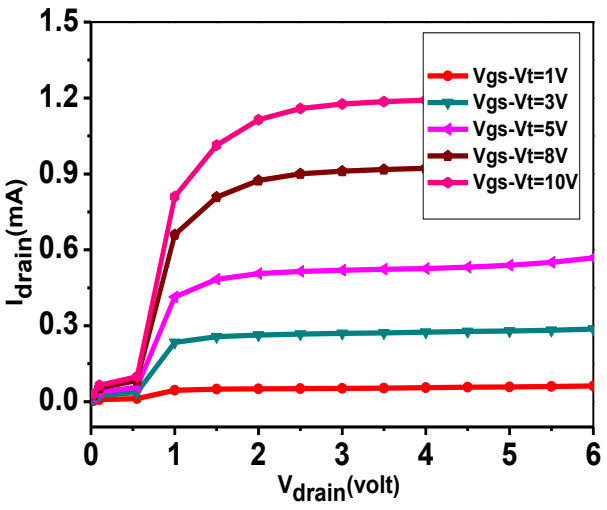

Fig. 3. IV characteristics of LDMOS transistor.

International Journal of Engineering Applied Sciences and Technology, 2016
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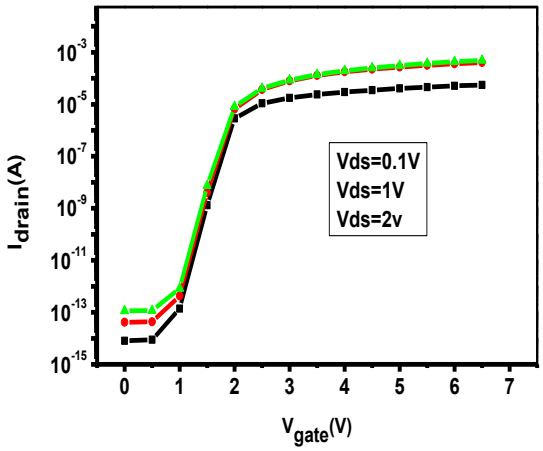

Fig. 4. Threshold voltage of LDMOS transistor .

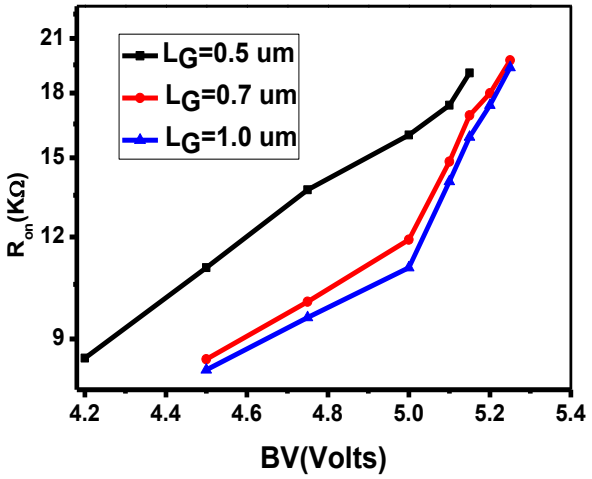

Fig. 6. A trade off between Ron & BV versus gate length.

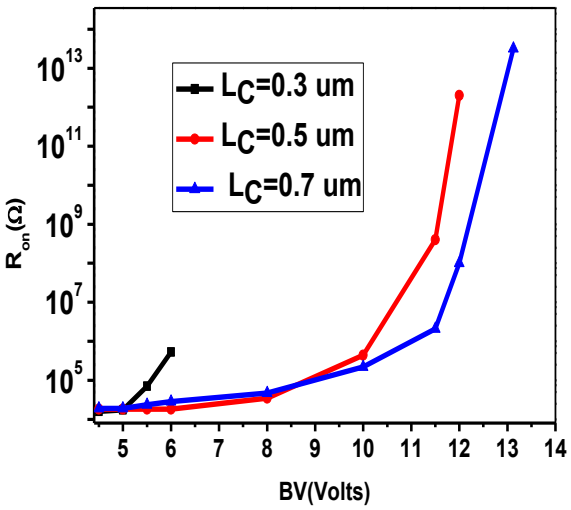

Fig. 5. A trade off between Ron & BV versus channel length.

parameter constant and R_{on} is calculated by the slope of the linear regime of the drain current-voltage (IV) characteristics (Fig. 3).

Several literatures reported that on resistance increases with the breakdown voltage as R_{on} is proportional to $BV^{2.5}$. The fig.5 and fig.6 show a tradeoff between R_{on} and BV with variation of channel and gate length keeping all other parameters constant. The on resistance and BV show trade off with varying gate and channel length at a gate voltage (V_{gs}) of 5V and drain voltage (V_{ds}) of 8 V. The fig.5 and fig.6 show that on resistance decreases with increasing gate length with different channel devices having length 0.3 um, 0.5 um and 0.7 um.

a. OUTPUT CONDUCTANCE

Fig.7 shows that the channel conductance decreases with increases the drain voltage, this is because as the drain voltage increases then the depletion width increases which reduce the channel hence conductance decreases and finally saturates when the device saturates.

The graph plots signify that drain conductance is almost constant with increase drain voltage. The O/P conductance (g_o) is proportional to drain current. Since drain current is almost constant in saturation region of LDMOS at higher drain voltage, g_o also becomes independent with increase drain bias.

b. Transconductance

Due to high Ron, LDMOS shows a low g_m. But g_m should be high because g_m is directly proportional to the o/p of amplifiers. Hence g_m has two attributes: peak gm range and gate voltage. Both should be higher for RF applications. So by reducing on resistance of device, peak g_m and range should be improved. In the saturation region, the transconductance (g_m) of LDMOS device is defined by following equation:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th}) = \frac{\partial I_D}{\partial V_{GS}} : V_{DS} = constt \quad (2)$$

Where,

Cox is the capacitance of gate, μ_n is the mobility of channel and L and W represents the length and width of the gate respectively. Fig.8, fig.9 and fig.10 show the g_m of the device which is defined by above equation. (Note: In LDMOS devices, g_m curve is reduced in the compression region due to low doped drain (LDD) region.

International Journal of Engineering Applied Sciences and Technology, 2016
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The g_m also gradually decreases after the peak because mobility of electron that gets reduced after the V_{DS} gets saturated. At high gate voltage, g_m decreases because channel mobility decrease and at low gate voltage g_m increases. These figures show the impact of illumination on g_m, the figures show that with enhance the V_{gs} the g_m increases this is due to the fact that with increase in the gate voltage, the depletion width decreases and the channel increases hence the conductance increases. For illumination there is increase in the conductance due to excess carriers generated. The peaks of transconductance are very well simulated by model which proves correct modeling of mobility behavior with transverse field and drift resistance.

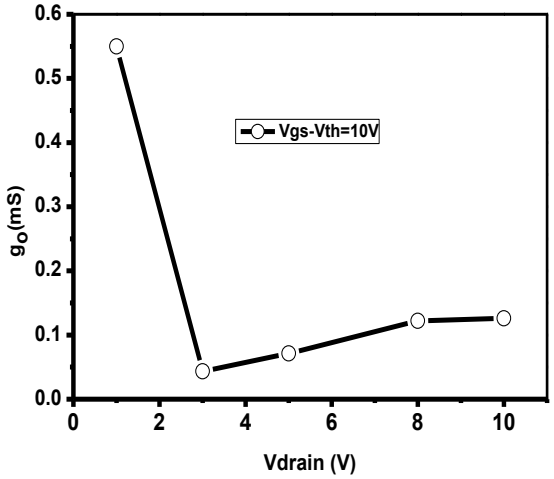

Fig. 7. Out put conductance at Vgs-Vth=10V with varying drain voltage.

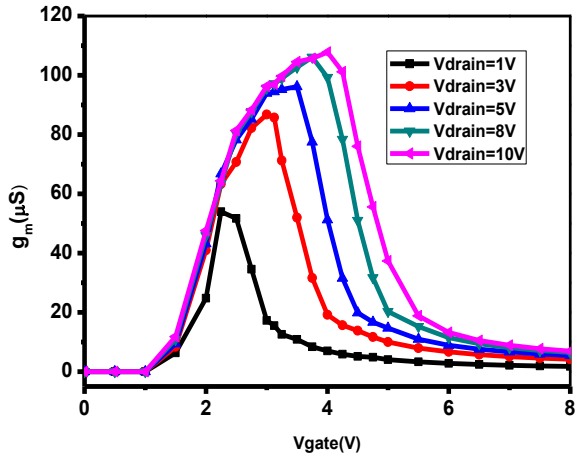

Fig. 8. A plot between transconductance and gate voltage with varying drain voltage.

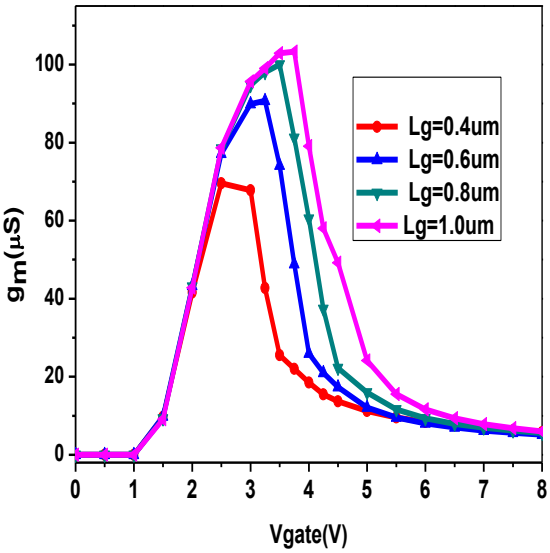

Fig. 9. A plot between transconductance and gate voltage versus gate length.

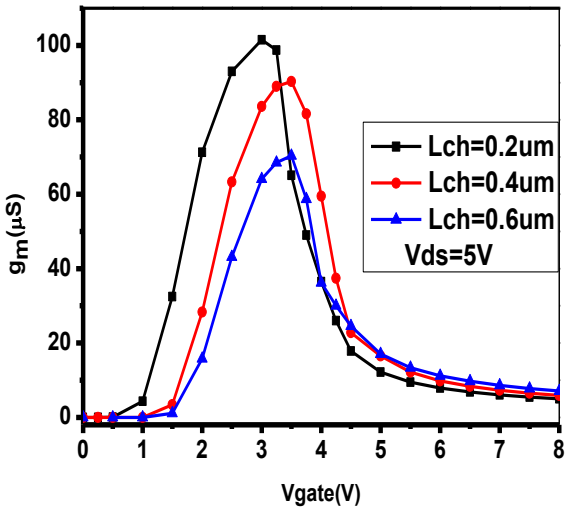

Fig. 10. A plot between transconductance and gate voltage with varying channel length.

The fig.8 plots of g_m at fixed drain voltage of 1V to 10V with varying gate voltage. The drain current is very small till device enters inversion region. The transconductance curve reaches a peak and then reduced due to influence of V_{gs} on effective mobility. The nature of plots of g_m are not similar for V_{ds}=1V to 10V. Because device are in linear region when drain voltage is low as 1V and device are in saturation region when drain voltage reaches at 10V.

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Vol. 1, Issue 4, ISSN No. 2455-2143, Pages 62-68
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Transconductance (g_m) is one of the very important factors considered in circuit design as it decides cut off frequency.

C. RF CHARACTERISTICS/AC ANALYSIS

AC analysis is performed to determine small signal characteristics of device. AC sinusoidal small signal analysis should be performed after solving for a DC condition.

In RF – transistor design, the frequency of operation is the main motive which depends on cut off frequency (f_t) and maximum oscillation frequency (f_{max}). Both are extracted through small- signal analysis. The f_t and f_{max} are the critical figures of merit for evaluating the performance of RF transistors. The f_t provides how rapidly a device can transfer charge in the channel from gate to drain. The cut off frequency and maximum oscillation frequency are related to transconductance and resistance.

Therefore the value of f_t depends on gate –source capacitance (Cgs) and trans-conductance (g_m) written in following equation;

$$f_T = \frac{g_m}{2\pi(C_{GD} + C_{DS})} \quad (3)$$

And f_{max} is the unilateral power gain (U) of the device:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{GD}}} \quad (4)$$

The cut off frequency and maximum oscillation frequency have been extracted by current gain (h_{21}) and unilateral power gain. When both is unity or have a magnitude 0dB.

The current gain and unilateral power gain have been calculated and plotted versus frequency. Fig.11 and fig.12 show the current gain and unilateral power gain with variation of V_{ds} at same gate and channel length.

The substantial rise in f_T can be contributed to enhance in drain current and hence transconductance have been improved. Fig.13 and fig.14 show the frequency response (f_t and f_{max}) versus gate length and channel length. The simulation was done at V_{ds}=5V and Vgs=10V. The equation (4) is applicable only for plot shown in fig. 13 because f_{max} has been degraded with enhance of gate resistance/ increase of gate resistance.

High frequency operation in LDMOS is achieved by short channel. A short channel makes the device operate in velocity saturation mode. The fig. 14 shows the plot f_t and f_{max} versus channel length. The result shows that f_t increases with gate length and channel length decreasing but same trend is not observed for f_{max}. The highest cut off frequency of 21 GHz is extracted for the device

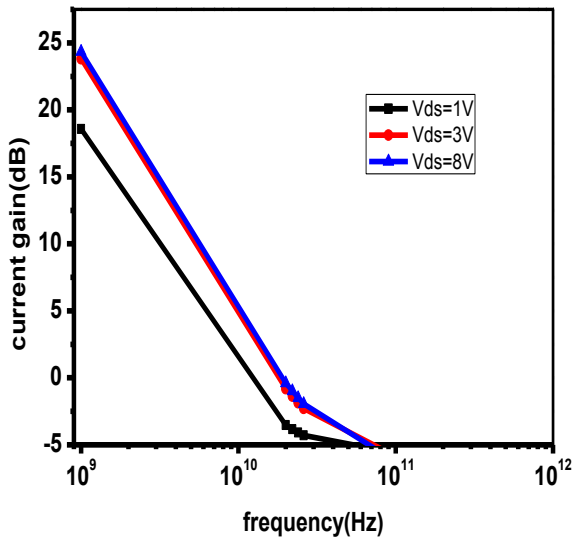

Fig. 11. Current gain vs frequency at different drain voltage.

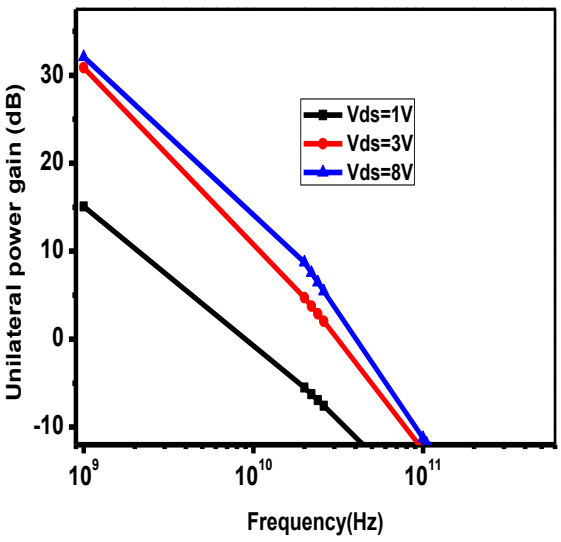

Fig. 12. Unilateral power gain vs frequency at different drain voltage.

at gate length 0.2 um. The f_{max} is strongly depend on parasitic components of LDMOS transistor like as gate drain and drain source capacitance or gate resistance. The value of f_{max} can be approximately expressed as follows:

International Journal of Engineering Applied Sciences and Technology, 2016
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$$f_{Max} = \frac{f_T}{\sqrt{4R_g\left(g_{ds} + 2\pi f_T C_{gd}\right)}} \quad (5)$$

In our work, f_{max} is probably related to the high output conductance (g_{ds}). The value of f_{max} is inversely proportional to g_{ds}.

In plot 14 f_{max} increases with decrease of drain resistance (R_D). When channel length increases then lightly doped drain region (LDD) reduced hence drain resistance also reduced. So equation (5) is applicable only for plot 14.

At high frequencies, a transistor with high f_t and f_{max} will have a low noise figure. In 0.3um LDMOS, f_t and f_{max} is expected to be 20 GHz and 50 GHz, respectively.

In RF transistor f_{max} is always higher than f_t. The f_{max} may be higher or lower than f_t. Transistor with fmax>f_t can have useful power gains also at frequencies above ft and up to f_{max}.

A simplified explanation for this is that the current gain lesser than one is compensated by a voltage gain greater than one in the frequency range between f_t and f_{max}. Thus, a power gain greater than one is possible. Transistors with f_{max}<f_T, however, can achieve power gain only at frequencies up to f_{max} and cannot be used as power amplifiers at frequencies between f_{max} and f_T. In the case of bipolar RF transistors, there existed a tradeoff between f_T and f_{max}. A bipolar transistor designed for maximum f_T commonly shows a relatively low f_{max} and vice versa.

A frequently asked question is which of the two characteristic frequencies, f_T and f_{max}, is more important for RF transistors. There is no unequivocal answer. The commonly cited statement that f_T is the more important FOM for digital circuits while for analog applications f_{max} is most significant is far too simple. The importance of f_T and f_{max} depends on the specific application of the transistor. Manufacturers of RF transistors often strive for $f_T \approx f_{max}$ so that the devices are useful for a large number of different applications.

Another important issue is that of the maximum operating frequency fop of an RF transistor with certain f_T and f_{max}. Again, there is no definite answer. A rather conservative rule of thumb is that both f_T and f_{max} of the RF transistor should be at least ten times higher than the operating frequency of the system in which the transistor is to be used. A less stringent requirement is that the operating frequency of an RF system should not exceed 50% of the cutoff frequency of the transistors used [13]. For power transistors, f_T must be at least equal to fop and f_{max} should be at least three times that of fop [14]. Clearly, the requirements differ from application to application

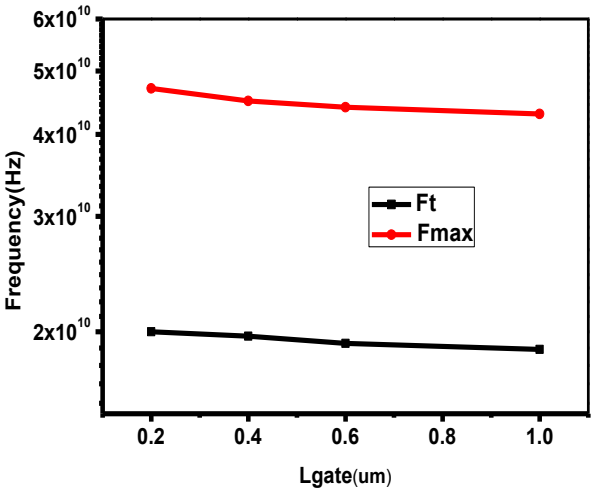

Fig. 13. Cut off frequency and Fmax vs gate length at Vds & Vgs-Vt=10V

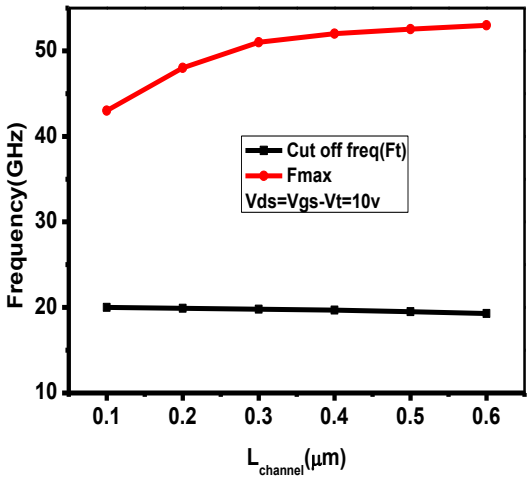

Fig. 14. Cut off frequency and Fmax vs channel length at Vds & Vgs-Vt=10V

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IV. CONCLUSION

In this paper, a LDMOS device has been proposed and investigated by simulation. This simulation results show the better RF characteristics. Optimization has been achieved by varying gate length and channel length. The variations of gate and channel length affect the all parameters breakdown voltage, on resistance and transconductance etc.

Breakdown voltage and Ron are 13.65V and $10^{13}\Omega$, respectively. By scaling the gate length and channel length,

our simulation revealed better improvement in all investigating parameters. The results of RF measurement for cut off frequency and f_{max} for device with different gate and channel length are simulated.

The simulation results have revealed; the 0.3 µm channel LDMOS device has better performance because of difference in device level process optimization and with gate length shorter than 0.3 µm lengths, device is difficult to secure leakage suppression.

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