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COMPARATIVE STUDY OF CMOS FRACTIONAL-N SYNTHESIZER BASED ON PHASE LOCKED LOOP- A REVIEW

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***Abstract*—In the area of communication and wireless system PLL plays an important role for the frequency synthesizers. CMOS fractional-N synthesizer that mainly depend on PLL (phase looked loop). PLL has various application in many areas such as in frequency synthesizer, phase modulation and demodulation, frequency modulation and demodulation, data and clock recovery circuit as well as in tacking filters. The stability and the tuning range of these synthesizers mainly based on PLL. Comparison on different type of frequency synthesizers such as fractional–N synthesizer are presented and different type of parameters for the fractional- N synthesizers such as spur, power dissipation, loop bandwidth, switching speed, lock in range and phase noise are defined for the fractional-N synthesizer.**

Keywords—**Fractional-N Synthesizer, PLL (Phase locked loop), CMOS (Complementary metal oxide semiconductor), voltage control oscillator, Integer-N Synthesizer.**

I. INTRODUCTION

An electronic circuit is generally required in order to get a range of frequency from the single frequency that is called recurrence synthesizers. The recurrence synthesizers are of two kinds Integer-N and Fractional-N synthesizers. Integer- N Synthesizers is conventional synthesizers where small input frequency is applied as an input or reference frequency. The channel spacing is also small in the integer-N synthesizers. Synthesizer configuration has demonstrated a troublesome undertaking for a considerable length of time, producing many RF combination methods. RF synthesizers commonly utilize stage locking loop. The conventional synthesizer [1] is given in fig1. In integer-N synthesizers, the yield channel dividing is equal to the reference recurrence. To get the better results of various parameters such as channel spacing, loop bandwidth, resolution and fractional spur fractional-N recurrence is presented. Different field of fragmentary N synthesizers has presented many procedures in the previous a very long while. Sigma delta fractional-N recurrence synthesizers have gotten well known for spectral purity applications since it gives fine recurrence resolutions for accomplishing low stage turbulence [3-5]. In the sigma delta fragmentary-N recurrence [2, 6, 7], the false presentation is improved through sigma delta adjustment by the Flip Flops. Quantization turbulence presented by Dithering the partition value of high frequency is formed, with the goal that it is considerably separated by the synthesizer elements. The formed quantization noise consistently directions at high frequencies Parity, that representing a high noise data transmission exchange off, which means closed loop move speeds for less stage turbulence synthesizers. The exchange off reasonably disregard the focal idea behind fragmentary N synthesizer, which generally extend synthesizer information transmission also, besides in the sigma delta incomplete N synthesizer, fallen turbulence adds to the in-band organize turbulence [3] in view of nonlinearity in loop. As of late, techniques dependent on divider-less PLL have likewise been proposed. Divider-less PLL structures, which include sub sampling PLL [8] and injection locked PLL [9-13], have accounted for accomplish better stage turbulence than the customary PLL models. In the partial infusion locking technique abuses the multiphase yields of a oscillator in form of ring for better repeat goals, anyway the fragmentary number can't be optional concerning the foreordained number of the times of the oscillator. To gain the superior goals, the hardware must be extended exponentially [6]. In spite of the way that a bit of uncovered all-computerized PLLs can perform partial N blend, they require incredibly exact TDCs and must be manufactured in CMOS advancements [7], [8]. Fractional –N synthesizers contain many blocks that are phase recurrence detector, current sink source, filter section II consists of literature study. Section III defines the basic blocks of PLL synthesizer design of circuit for different fractional-N synthesizers. Section IV defines the various architecture of fractional-N synthesizer. Section V defines the various performance parameters of the fractional-N synthesizers. Section VI defines the comparison table of different fractional-N Synthesizers performance parameters for the

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previous research works. Section VII defines the conclusion of this presented work.

II. LITERATURE STUDY

S-Y yang et.al [25] describe all advanced recurrence synthesizers with powerfully reconfirmed digital loop in 90nm cmos technology. The various performance variables such as power scaling, locking speed and division ratio improved. It could be achieved by dual mode phase and frequency detection scheme.

Ebrahim et.al [24] describe the wideband fractional-N synthesizer is proposed based on 0.18um cmos technology. This structure used synthesizers which is very simple and having low power consumption and low output jitter.

C. hsu et.al [17] describe the digital fractional-N frequency synthesizer which is implemented using 0.13um cmos technology. This architecture used GRO-TDC.

Chan Yang et.al [21] proposed a fractional synthesizer which is based on scheme i.e. automatic frequency calibration (AFC). The AFC circuit applied to cmos recurrence synthesizers which quantifies the lock time. It is implemented using 0.18um cmos technology.

Pyoung Won et.al [22] defines a fractional-N Synthesizers that depends on offset phase locked loop [OPLL]. This synthesizer implemented using 0.13um cmos technology. It accomplishes 9 db of noise decrease when contrasted with ordinary PLL and consumes 3.2mw power.

III. BASIC BLOCKS OF PLL SYNTHESIZER

Fig 1 defines the conventional synthesizers which comprises of different blocks, for example PFD (phase and recurrence indicator), charge pump, low pass filter and voltage controlled oscillator (VCO) and multiplier.

The Function Performed by the various blocks are as follows:

A. **PFD (phase and frequency detector)** –

This detector generally used for comparison between signals that is the feedback signal and the input signal or reference signal that is applied to the input. The output is generated that is phase difference of the two signal .It is also known as phase error. The stage recurrence indicator (PFD), which helps PLLs accomplish synchronous stage and recurrence blunder recognition, is a key practical square and assumes a significant job in improving the presentation of the entire PLL framework [14].

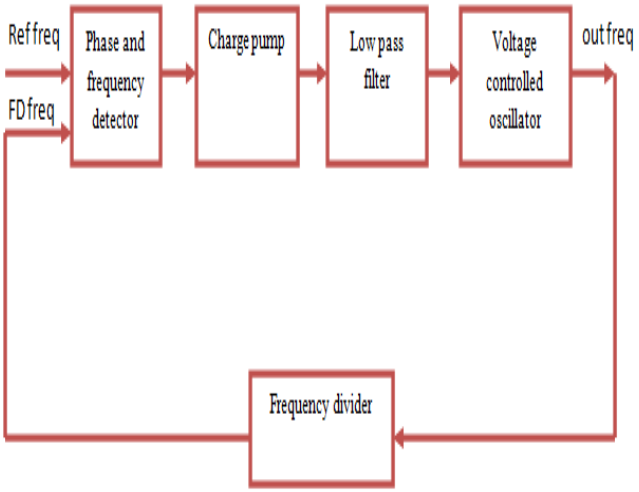

Fig.1. Conventional Synthesizer

B. **CP (Charge pump)** –

The PFD generates the two signals up signal and down signal which are generally applied to the CP which produces control signal which is to be applied across the loop filter.

C. **Passive low pass Filter** –

Loop filter is basically a filter which improves the stability and is required for removing unwanted frequency component from the PFD. The oscillation produced by the VCO depends on the output of filter. Various parameters get affected like stability, loop bandwidth and phase noise.

D. **VCO (voltage controlled oscillator)** –

The yield of the low pass channel gives the voltage which is essential for generating the frequency of oscillator for the voltage controlled oscillator. Different types of oscillator can be used for the VCO such as LC and Rind oscillator. LC oscillator have certain drawback that the adjustment range is small and cost is high as well as power consumption is high, so generally Ring oscillator is used in which odd number of

delay stages are used. So that it forms a ring around the loop. Thus, VCO plays an important role in the frequency synthesizers. Its functioning depends on the charge pump. Charge pump is mainly responsible for generating the control voltage which generally increase or decrease the frequency. The delay cell [15] and ring oscillator utilized in the synthesizer. LC-tank oscillators have indicated great stage turbulence. Be that as it may, there are a few weaknesses. To start with, the tuning scope of a LC is generally low when contrasted with ring oscillators. The yield recurrence may drop out of the ideal range within the sight of procedure variety. Second, the stage turbulence execution of the oscillators profoundly relies upon the quality factor of on-chip winding

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inductors. For most advanced CMOS forms, it is hard to get a quality factor of the inductor bigger than three. In this manner, some additional preparing steps might be required. At last, on-chip winding inductors possess a ton of chip zone, which is unfortunate for cost and yield contemplations. Ring oscillators can be effectively incorporated on-chip with no additional preparing steps. Ring oscillators regularly possess less chip region, which improves both the yield and the expense.

E. **Frequency Divider** –

Frequency divider plays significant job in the fractional-N Synthesizers. The series of flip flops are used to generate the frequency divider.

IV. VARIOUS ARCHITECTURE ARE USED IN THE PREVIOUS RESEARCH FOR THE FRACTIONAL-N SYNTHESIZERS

Some of which are as follows-

A. **Architecture proposed by HOSSEINI et.al [2019]** –

In this paper a synthesizer is proposed which is simple. It is based on analog PLL architecture having the reference frequency is 50hz and output frequency is (2.1- 2.5) GHz. The bandwidth is 5MHZ and power consumption is 36mw. This architecture is executed using 0.18um cmos process. FVC used in loop 2 is presented [24].

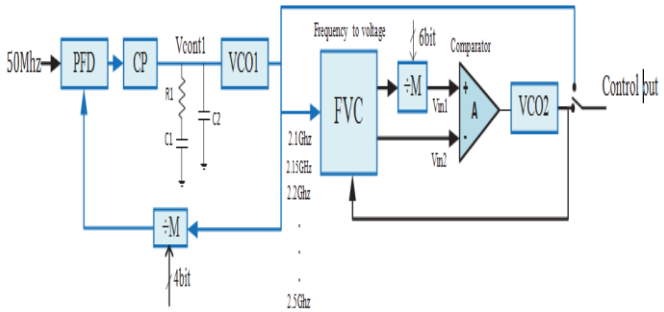

Fig.2. Fractional-N Synthesizer Based On Analog PLL

B. **Architecture proposed by Jeong et.al [2009]** –

A fractional-N synthesizer proposed with the automatically frequency calibration scheme. This design is executed utilizing 0.18um cmos process possess the area 0.01mm^2. The phase noise in this comes out to be -113dbc/Hz at 1MHZ. Power utilization in this architecture is 23mw from 1.8volt supply. The uncertainty of phase relationship is also eliminated with the two phase reference clock and VCO clock comparison [21].

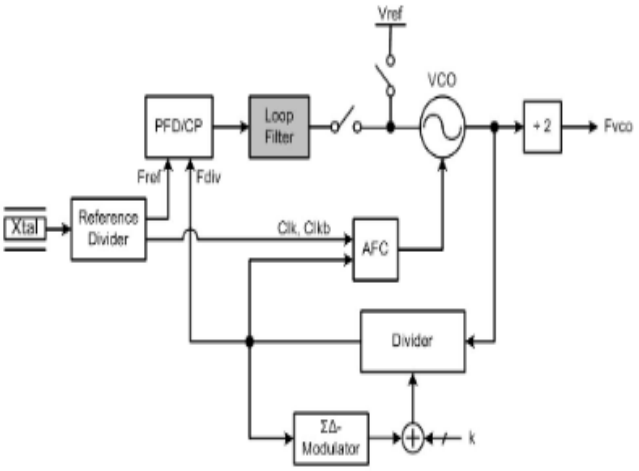

Fig.3. Fractional-N Synthesizer Based On AFC

C. **The Architecture proposed by Heng et.al [2003]** –

A 1.8 GHZ partial-N recurrence synthesizers is proposed which is actualized in 0.6um cmos. The spurious tones get eliminated with the multiphase vco. The power consumption is 52mw from a 3.3v. The phase noise is less than -80dbc/Hz within 20KHz loop bandwidth. The fine frequency resolution 1.8 GHZ is achievable and phase mismatch error with a multiphase VCO can be minimized [23].

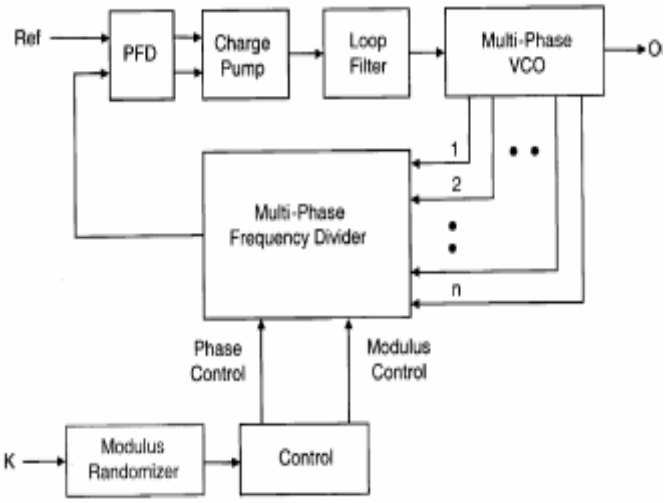

Fig.4. Multiphase VCO Fractional-N Synthesizer

D. **Architecture proposed by Hsu et.al [2008]** –

In this paper digital fractional-N frequency synthesizer is presented. It presents an architecture that utilizes a gated ring oscillator TDC with 6ps resolution. This design is actualized in a 0.13um cmos process having possesses 0.95mm^2 dynamic region. The power dissipation is 39mw for core parts and 8mw for oscillator output buffer. An interfacing is utilized, for example, DAC put between filter and VCO the noise comes

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out to be 3.67GHZ with a reference of 50MHZ achieves -108dbc/Hz and -150dbc/Hz at 400 KHz and 20 MHz offsets respectively [17].

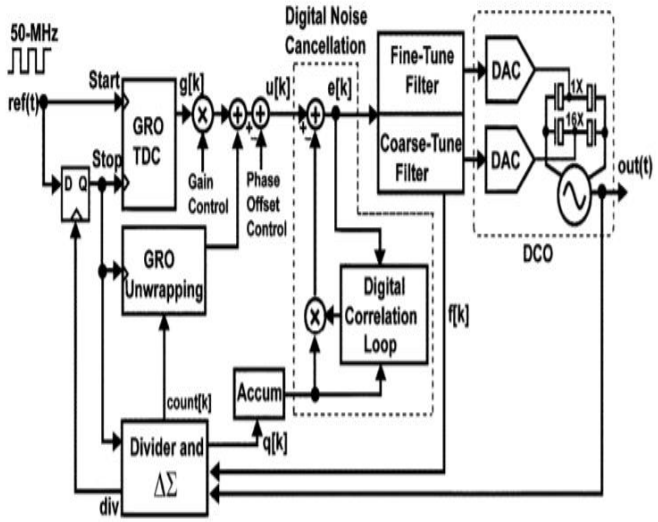

Fig.5. Digital Fractional-N Synthesizer

V. PERFORMANCE PARAMETER

There are different types of performance parameter which effects the fractional–N synthesizers such are as follows:

A. Fractional spur

B. Bandwidth

C. Phase noise

D. Lock in range

E. Switching speed

F. Power dissipation

A. **FRACTIONAL SPUR** –

In the fractional–N synthesizers, the voltage controlled oscillator produces the fractional spurs. The sidebands are generally called spurs. These spurs can be reduced by the following ways; -

A up/down skew reduction.

B up/down current mismatch.

C sampling loops filter.

B. **BANDWIDTH** –

For the consideration of noise, the 3db bandwidth is considered. It takes two parameters Natural frequency (w_n) and Damping ratio (ξ) for 3db Bandwidth. 3db bandwidth can be given as:

$$w_{3db}=2\xi w_n \text{ for } \xi=0.707(\xi<1)$$

$$=2.5w_n \text{ for } (\xi=1)$$

$$w_{3db} = \left(1 + 2\xi^2 + \sqrt[2]{(1 + 2\xi^2)^2 + 1}\right)^{\frac{1}{2}}$$

C. **PHASE NOISE** –

The performance of the fragmentary–N synthesizers relies upon the stage noise. Hence it is the main parameter for the system. Another name for the phase noise is phase jitter. The phase noise can decrease by keeping the Bandwidth as large as possible.

D. **LOCK IN RANGE** –

locked state is frequency range so that the phase error remains constant or zero. Which is estimated between the yield of the VCO and the reference signal. To remain the phase error constant a control mechanism is generally used for the synthesizers.

E. **SWITCHING SPEED** –

Switching speed is the switching time or settling time. It defines how the output logics states changes in order to get output for its changing input state under the certain condition.

$$T_S = \frac{4}{\xi w_N}$$

F. **POWER DISSIPATION** –

Power utilization is the one of important parameter. It is the biggest challenge as we deal with the very large scale integration (VLSI). It must be as small as possible for the given voltage supply. Low power consumption has many advantages. Power must be optimized for the satisfied results in the research work.

VI. COMPARISON TABLE

Different architecture of fractional-N PLL synthesizers and its performance parameters are studied. The comparison of different fractional-N synthesizers can be explained as by the following comparison table.

Table -1 Comparison Of Different Fractional-N Synthesizers

Design	[17]	[18]	[19]	[20]	[9]	[24]
Process (um)	0.13	0.18	0.13	0.18	0.9	0.18
Architecture	GRO-TDC	Sub-sampling	DPLL	Analog PLL	ADPLL	Analog PLL
Reference (MHz)	50	48	64	12	25	50
Output range (GHz)	3.62-3.67	2.12-2.4	2	2.4-2.5	1.6-1.8	2.1-2.5
Phase noise (dBc/Hz)	-108	-112	-107	-98	-116	-105
Lock time	NA	25ms	NA	NA	NA	500ns
Bandwidth	500KHz	500KHz	1MHz	975KHz	0.4-0.8MHz	5MHz
Power(mw)	46.7	17.3	21	49	121	36

VII. CONCLUSION

Study of various Fractional-N PLL Synthesizer and comparative analysis of performance parameter is done. Analog PLL [24] presented better lock time and bandwidth as compared to other architecture. In the DPLL [19] have better power dissipation. The architecture GRO-TDC depicts improved output frequency range [17] and better tuning range.

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