



IJEAST

INTERNATIONAL JOURNAL
OF ENGINEERING APPLIED SCIENCE
AND TECHNOLOGY



VOLUME : 4 ISSUE : 03 Print / Issue Publication Date: 02-Sep-2019



ISSN : 2455-2143



DOI : 10.33564/IJEAST.2019.v04i03.087

Indexed In



WWW.IJEAST.COM

editor@ijeast.com



Comparison of Power Estimation Between Reversible & Irreversible Logic Gates

Subham Chowdhury
Department of Physics
The University of Burdwan
Burdwan, India-713104

Sarupya Chowdhury
Department of ECE
Supreme Knowledge Foundation
Group of Institutions
Mankundu, India-712139

Sauvik Mondal
Department of ECE
Supreme Knowledge Foundation
Group of Institutions
Mankundu, India-712139

Sayantana Bose
Department of ECE
Supreme Knowledge Foundation
Groups of Institutions
Mankundu, India – 712139

Debjani Basu
Department of ECE
Supreme Knowledge Foundation
Group of Institutions
Mankundu, India - 712139

Abstract– In this article, basic irreversible gate (XOR gate) and basic reversible gates are designed using dataflow design. The output of all the basic gates are simulated and compared the power in Analyze power (Xpower) compiler. The combinational circuits (adder and subtractor) and sequential circuit (T flip flop) are designed using structural design with both conventional logic gates and reversible logic gates and power has been measured. Overall the power of conventional logic gates and reversible logic gates are compared that helps us to design gates with less power dissipation and more efficiency. All the individual reversible logic gates and complex combinational and sequential circuits are described in VHDL hardware description language and this circuits are functionally verified using Xilinx ISE 9.1i (student version) software.

Keywords– Reversible logic gates, power analysis, less power dissipation, VHDL

I. INTRODUCTION

Gordon. E. Moore et al. (1965) predicted that the numbers of components on the chip will double every 18 months. Initially he predicted only for 10 years but due to growth in the integrated-circuit technology his prediction is valid till today [2]. His work is widely recognized as the Moore's law. The effect of Moore's law was studied carefully and researchers have concluded that as the number of components in the chip increases the power dissipation will also increase tremendously. It is also predicted that the amount of power dissipated will be equal to the heat dissipated by the rocket nozzle. Landauer et al. stated that

the amount of energy dissipated to erase each bit of information is at least $kT \ln 2$ (where k is the Boltzmann constant and T is the room temperature) during any computation the intermediate bits used to compute the final result are erased [1]. This erasure of bits is one of the main reasons for the power dissipation. C.H. Bennett (1973) revealed that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model [10]. The most prominent application of reversible logic lies in quantum computers. It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing [7].

II. DESIGN OF BASIC LOGIC GATES

XOR gate- a logic irreversible gate and NOT gate (1*1), CNOT gate (2*2), Feynman Gate (2*2), Toffoli gate (3*3), Fredkin gate (3*3), Peres gate (3*3)- some reversible logic gates are designed using dataflow design of VHDL hardware description language and verified using Xilinx ISE 9.1i (SV) software [4-6].

Table 1. Truth table of XOR gate

Input		Output
A	B	P
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 1. Waveform of XOR gate





Table 2. Truth table of NOT gate

X	Z=X'
0	1
1	0

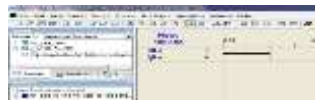


Fig 2. Waveform of NOT gate

Table3. Truth table of CNOT gate

X	Y	X'	Y'
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0



Fig. 3. Waveform of CNOT gate

Table 4. Truth table of Feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0



Fig. 4. Waveform of Feynman gate

Table 5. Truth table of Toffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0



Fig. 5. Waveform of Toffoli gate

Table 6. Truth table of Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	1



Fig. 6. Waveform of Fredkin gate

Table 7. Truth table of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0



Fig. 7. Waveform of Peres gate

III. DESIGN OF COMBINATIONAL AND SEQUENTIAL CIRCUIT

A. COMBINATIONAL CIRCUITS-

Adder and subtractor are taken as example of combinational circuits. Combinational circuits consist of some basic logic gates. Full adder using irreversible logic gates consist of Half adder and OR gates, whereas reversible logic gates consist of Peres gates. In the other hand, Full subtractor using irreversible logic gates consist of Half subtractor and OR gate, whereas reversible logic gates consist of TR gates. This all gates are designed using structural design of VHDL hardware description language and verified using Xilinx ISE 9.1i (SV) software [8].

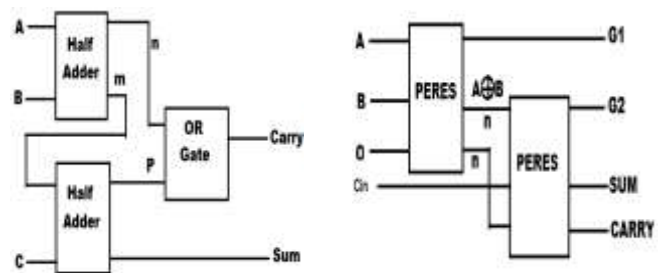


Fig. 8. Block diagram of Full adder using a. irreversible logic gates b. reversible logic gates

Table 8. Truth table of Full adder

Input			output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 9. Truth table of Full subtractor

Input			output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Fig. 10. Waveform of Full adder a. irreversible logic gate b. reversible logic gate



Fig. 12. Waveform of Full subtractor a. irreversible logic gate b. reversible logic gate

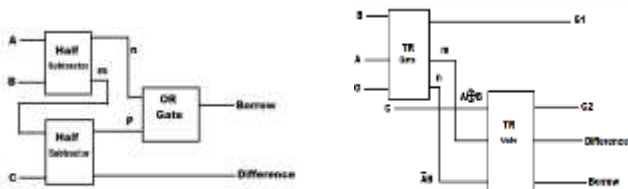


Fig. 11. Block diagram of Full subtractor a. irreversible logic gate b. reversible logic gate

B. SEQUENTIAL CIRCUITS

Sequential circuits consist of some basic logic gates. Here T flip flop is taken as an example of sequential circuit. This T flip flop is made of two reversible logic gates SG gate and FG gate. This T flip flop is designed using structural design of VHDL hardware description language and the truth table is verified.

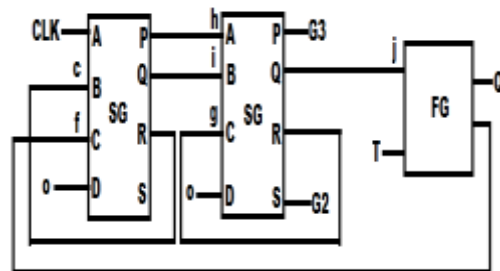


Fig. 13. Block diagram of T flip flop

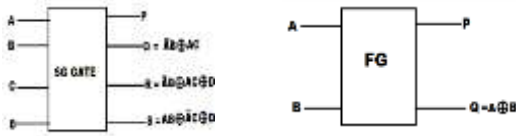


Fig. 14. Block diagram of SG and FG gates

Table 10. Truth table of T flip flop

T _n	Q _{n+1}
0	Q _n
1	Q _n

IV. POWER ESTIMATION

Now, the power of all irreversible and reversible gates (basic gates, combinational circuits and sequential circuit) are compared in Analyze power (Xpower) compiler [8] and presented in the table below.

Table 11. Power calculation for Irreversible & Reversible Gates

Power Estimation		
Different Types of Gates	Normal Logic	Reversible Logic
Basic Gates	23.50 mW	17.50 mW
Combinational Circuits	23.50 mW	17.50 mW
Sequential Circuits	25 mW	17.50 mW

V. CONCLUSION

Matter of concern in this article is to reduce the power and to increase the efficiency. The goal is achieved by using reversible logic gates in basic gates, combinational circuits and sequential circuit. Here it can be seen that the power is increasing in complex circuits for normal logic, whereas the power is fix at a certain value for reversible logic gates. So, it can be used for complex circuits in quantum computing CMOS design nanotechnology etc.

In this article the power is analysed in Xilinx ISE 9.1i (SV) software[8] but if Cadence software[9] is used it will give more accurate results.

VI. REFERENCES

- [1] Landauer, R., "Irreversibility and heat generation in the computing process", IBM 1.Research and Development, 5(3): pp. 183-191, 1961.
- [2] A. P. Chandrakashan, S. Sheng, and R. Brodersen, "Low power CMOS digital design," IEEE J. Solid-State Circuits, vol. 27, pp. 473483, Apr. 1992.
- [3] T.Toffoli, "Reversible Computing" Tech memoMIT/LCS/TM-151, MIT Lab for Computer Science 1980.
- [4] Fredkin E. Fredkin and T. Toffoli, "Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982
- [5] Peres, "Reversible Logic and Quantum Computers", Physical review A, 32:3266- 3276, 1985.
- [6] R. Feynman, "Quantum Mechanical Computers", Optic News, Vol 11, pp 11-20 1985.
- [7] D.Maslov and G. W. Dueck, "Reversible Cascades with Minimal Garbage", IEEE Trans on CAD, pp.1497-1509, 2004.
- [8] www.xilinx.com
- [9] www.cadence.com
- [10] C.H. Bennett, "Logical Reversibility of Computation", IBM J. Research and Development, pp. 525-532, November 1973.
- [11] M. Mohammadi and M. Eshghi, "On figures of merit in reversible and quantum logic designs", Quantum Information Processing,8(4):297318, Aug. 2009.
- [12] M. Saravanan, K. Suresh Manic, "Energy Efficient Code Converters using Reversible Logic Gates", International Conference on Green High-Performance Computing, IEEE, pp. 1-6, March 14-15, 2013.
- [13] Kotaiah Kamani, Sandeep Koneti, Ujwala Bollampalli, Sreevani shankara, "Energy Efficient Reversible logic Design for Code converters", ICETET , vol. 1, issue 3, pp. 132-136, July-Sep 2014

IJEAST

INTERNATIONAL JOURNAL
OF ENGINEERING APPLIED SCIENCE
AND TECHNOLOGY

ABOUT IJEAST

International Journal of Engineering Applied Science and Technology (IJEAST) is a peer-reviewed, open access journal that publishes high-quality research papers in the field of Engineering, Applied Science and Technology.

IJEAST aims to provide a platform for researchers, academicians, and professionals to share their innovative ideas, research findings, and practical experiences with the global scientific community.

FOCUS AREAS

- Engineering
- Applied Science
- Technology
- Innovation & Development
- Interdisciplinary Studies



PEER REVIEWED

All submissions are rigorously peer reviewed to ensure quality.



OPEN ACCESS

Free and unrestricted access to research for all.



GLOBAL REACH

Connecting researchers and professionals worldwide.



TIMELY PUBLICATION

We ensure a swift and efficient publication process.



For more information, visit our website

www.ijeast.com



INTERNATIONAL JOURNAL
OF ENGINEERING APPLIED SCIENCE
AND TECHNOLOGY

✉ editor@ijeast.com

🌐 www.ijeast.com

📍 India



2455-2143