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A COMPARATIVE STUDY OF VARIOUS SRAM CELLS

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Abstract—**The development in computerized gadgets has led to a huge increment in their presentation. To satisfy these needs, essential memory is required. Developments in memory innovation are reflected with regard to high density, fast processing speed, and rapid and low energy memory cells. Consequently, fast processing speed, low power and high reliability are significant worries in structuring SRAM cells. Bringing down the voltage, meets the low control specification of the device and yet builds the delay and diminishes security. In this manner, there is an exchange occur between the stability parameters. Based upon the specific application and different strategies, for example, scaling gadget size, voltage, are utilized to enhance the general execution of the memory cell. This paper thinks about several structural plans of SRAM topology, for 6T, 7T, 8T and 9T SRAM based on power dissipation, SNM and delay.**

Keywords— **Read delay, Write delay, Power dissipation, WSNM, RSNM.**

I. INTRODUCTION

Interest for battery work, fast compact gadgets for example, scratch pad, smart phones, desktop computers and so on increment step by step. High speed compact gadgets require primary memory that reacts rapidly. Due to this, SRAM is used, which is fast and refreshing does not need to be repeated. In fast speed SRAM cells, leaking of current and dissipating of power are the major concern which makes the life of the battery short. Therefore, these parameters should be low while making the design of SRAM cell.

The supply voltage is expanded within range to keep up power consumption. Power density within range can be maintained that is need for power sensitive application. Circuit strategy and framework stage procedures with power supply scaling are additionally required to accomplish low power plan [1]. Forceful scale down the gadgets not just increments sub-threshold leakage yet additionally has another adverse impact [2]. A little change in channel lengths may have enormous edge voltages variety, which makes hardware attributes not realizable. To neglect these tiny channel impacts, oxide thickness scaling, higher and uneven doping should be consolidated [3]. Low oxide thickness offers high electric field, gives the result in reliable direct tunneling current [4]. A multi-threshold CMOS technology works in rest mode and active mode, which diminishes static dissipating power of SRAM cell [5, 6]. In other strategy to enhance the SRAM accuracy and dependability, a low region body biasing circuit is designed [7].

In VLSI scaling various gadgets are turning into a significant leakage peripheral for such applications like embedded cache, battery controlled systems where leakage current should very low. Hence, leakage current is a significant problem in scaled innovation.

This paper is arranged as follows: Section II is about literature review of past studies. Some performance parameters are talked about in Section III. Section IV draws the comparison tables. In the end, Section V defines the conclusion of this presented work.

II. LITERATURE REVIEW

A. *6T SRAM-*

T.H. KIM et.al. 2008 presented six transistor SRAM cell (figure 1) [8]. A circuit design of a traditional SRAM cell shows in which before the start of the read operation, bitbar line (BLB) and bit line (BL) are precharged to higher Vdd. At that point, the access transistors become ON with the selected word line. Depending upon the information stored in Q/QB, discharging takes place at BL/BLB which performs read and write operation.

Traditional six transistor SRAM cell [9] meets issues at low supply voltages. All things considered, on not high voltages, weak write-access transistors could not overcome the heavy feedback response of cell inverter. Hence, access transistors unable to implement the contribution in the input of the ideal cell in the write operation.

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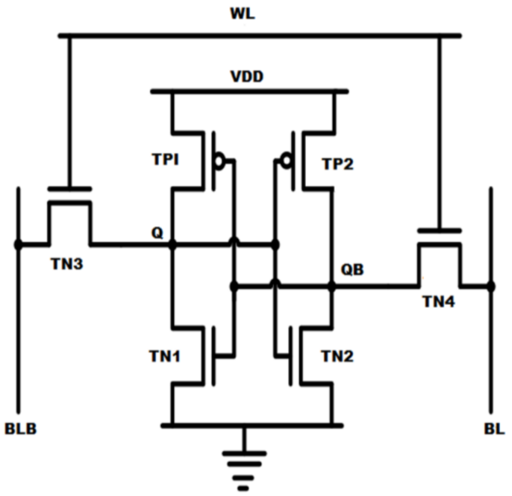

Fig. 1. 6T SRAM [8]

B. *7T SRAM –*

The design of seven transistor SRAM cell is consist of two CMOS inverters. Which are internally latched with the extra NMOS transistor that is associated with the read line and has two NMOS access transistors joined with bitline bar and bitline individually. From the given figure 2 of 7T SRAM, the M5 access transistor is attached with the word line (WL) which performs write operation and M6 transistor is joined to the read line (R). Throughout the read and write tasks, bit line operates as I/O nodes which convey the information to the sense amplifier [10].

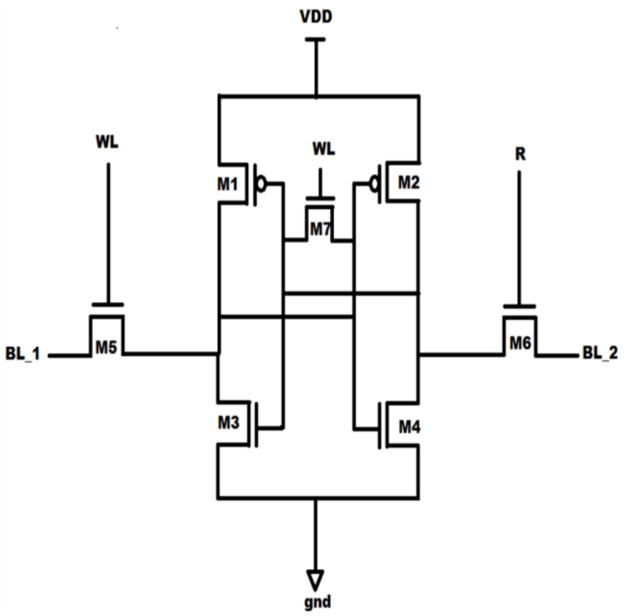

Fig. 2. 7T SRAM

C. *8T SRAM –*

G. Pasandi et.al. 2014 presented eight transistor SRAM cell. Circuit design of eight transistor SRAM cell [11] is demonstrate by figure 3. In given cell, M6 used as a read access transistor and M5 used as a write access transistor. Having independently working transistors in the given cell, it is achievable that the dimensions of the read transistor can be increased for enhancement of read operation and the dimensions of the write access transistor can choose to a minimum to improve the write operation. While in 6T SRAM, there is an issue when shaping the access transistor. In the given 8T SRAM cell, the extra M7 (pMOS) and M8 (nMOS) transistors are OFF throughout the write activity. Due to this, connections of VDD and GND are interrupted in the cell inverter.

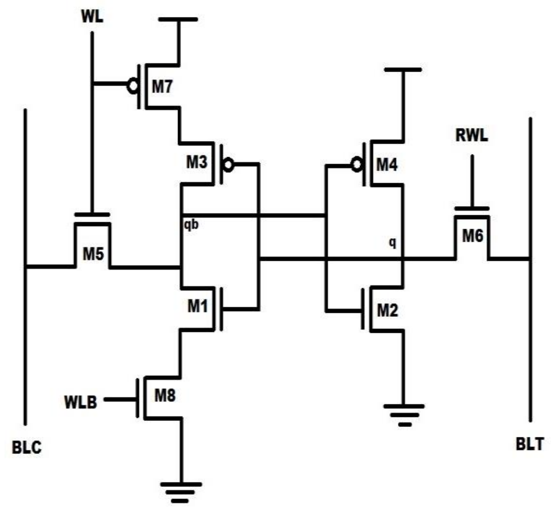

Fig. 3. 8T SRAM [12]

Kim et al. [12] used stronger working transistors by using reverse short channel effect [utilizing working transistors with greater channel length]. Another method to enhance the writing efficiency of traditional SRAM is to create a loop of feedback between cell inverters to weaken the cell and break this feedback loop throughout the write activity [13-16].

D. *9T SRAM –*

Z. Liu et.al. 2008 presented nine transistor SRAM cell [17] is appeared in figure 4. Write activity is alike to the six transistor SRAM cell. Read activity is done by N5, N6 and N7 separately which is handled by read signal (RWL). In 2011 A. Teman et.al. introduce 9T SRAM [18] cell executing supply feedback idea internally weakening the pull up current throughout the write operation thus uses low voltage. Additionally, various assisting of writing strategy like Vdd failure, negative bit-line, plugged Vss, wordline boosting strategy [19-23] introduced.

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To enhance the read stability, a nine transistor SRAM cell was introduced with different read port [24-25] and for enhancing write stability, negative bit-line strategy is used.

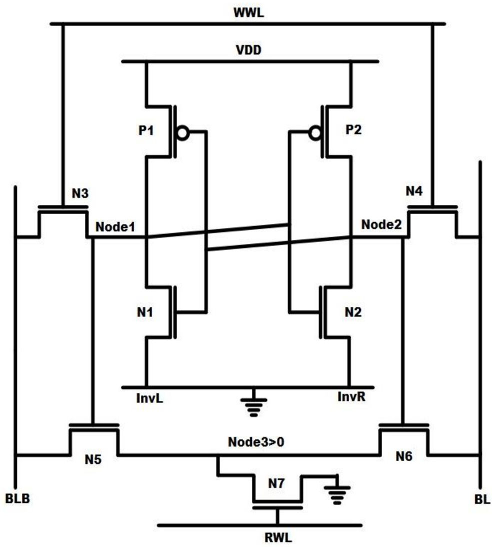

Fig. 4. 9T SRAM CELL [18]

III. PERFORMANCE PARAMETERS

There are different types of performance parameter which effects the various SRAM cell such are as follows.

A. *RSNM (Read-Static-Noise-Margin) –*

The tolerated DC noise (Vn) by pair of cross-coupled inverters present in data storing flip flop. This margin amount of DC noise is managed such that bitcell retains the data. VTC (Voltage Transfer Characteristics) gives the value of read SNM [26].

B. *WSNM (Write-Static Noise-Margin) –*

The WSNM is described by write trip point voltage, known as the greatest measure of voltage required on the bit line to flip the content on the bit cell [27, 28].

C. *Static Power Dissipation –*

Static power consists of leakage and standby power and also represents the type of consumption of power which is autonomous of movement. In off state region, transistor consumes the leakage power because of reverse bias current. The constant flow of current from Vdd to ground contributes in static and standby power.

D. *Write Delay –*

This is a considerate amount of delay among the two variables i.e. application of word line (WL) signal and data written moment.

E. *Read Delay* –

It is the delay between the reaction time of the sense amplifier and applications of WL signal. Also, read delay permits the bit line to discharge upto 10% of the peak value [29].

IV. COMPARISON TABLES

The various SRAM cells and its performance parameters are studied. The different SRAM cells are discussed on various CMOS technology. Table 1 compares the details of static power dissipation, WSNM and RSNM.

Table -1 Static Power Dissipation, WSNM and RSNM Comparison

SRAM Cells	Supply voltage (V)	Technology (nm)	WSNM (mV)	RSNM (mV)	Static Power Dissipation
6T [30]	0.6	65	160	190	310pW
7T [36]	0.6	90	406	120	NA
8T [33]	1	45	180	200	6.22nW
8T [34]	1	90	200	291	44.85nW
9T [26]	0.6	65	170	250	NA
9T [35]	0.6	65	228	225	240pW
9T [31]	1.2	65	270	210	NA
9T [38]	1.2	65	500	400	521nW

Table -2 Read and Write Delay Comparison

SRAM Cells	Supply voltage (V)	Technology (nm)	Read Delay	Write Delay
6T [30]	0.6	65	2ns	145ps
8T [34]	1	90	27ps	183ps
9T [26]	0.6	65	3.7ns	1.2ns
9T [35]	0.6	65	32ps	150ps
9T [31]	1.2	65	609ns	7.9ns

Table 2 express the comparison between the read and write delay at different voltages and technology node.

V. CONCLUSION

The various SRAM cells of different topologies are reviewed. At 65 nm technology node, RSNM and WSNM of 6T [30] SRAM cell is less than the 9T [26] SRAM cell. To get more RSNM in 6T SRAM cell, a pull down transistor could be used with a larger width. While 9T [38] SRAM cell has much greater WSNM and RSNM value as compare to 6T,7T, and 8T at 65nm technology node. Yet the area of the SRAM will also be increased which causes high leakage current. At 90 nm technology node, WSNM of the 7T [36] SRAM cell is larger than the 8T [34] SRAM cell. During write operation, this irregular design of 8T [34] SRAM cell is vulnerable to failure. Static power dissipation of 6T [30] SRAM cell is very less as compare to 7T, 8T and 9T using 65 nm technology node. While at same technology node, read and write delay of 9T [35] SRAM cell is better as compare to various SRAM cells discussed in this paper. Dual-threshold voltage approach can be used to lower down the delay and static power dissipation [37].

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