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DESIGN AND IMPLEMENTATION OF 8 BIT AND 16 BIT ALU USING VERILOG LANGUAGE

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***Abstract*: In this Paper present Arithmetic and Logical Unit (ALU) using HDL Verilog Language. An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logical operations. It represents the fundamental component of a computer's CPU. Modern processors contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). In this Paper presented the 8 bit and 16bit ALU architecture and its implementation using Verilog Language.**

Keywords: **ALU, CU, CPU, HDL, VLSI**

I. INTRODUCTION

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logical operations. It represents the fundamental component of a computer's CPU. Modern processors contain very powerful and complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU).

Most CPU operations are performed by one or more ALUs, which load data from the input registers. A record is a small amount of storage available as part of a CPU. The control unit tells the ALU the operation that will be performed on this data and the ALU stores the result in an output record. The control unit moves the data between these registers, the ALU and the memory.

An ALU performs basic arithmetic and logic operations. Examples of arithmetic operations are addition, subtraction, multiplication, and division. Examples of logical operations are comparisons of values such as NOT, AND, and OR.

All the information in a computer is stored and manipulated as binary numbers, that is, 0 and 1. Transistor switches are used to manipulate binary numbers because there are only two possible states. A switch: open or closed. An open transistor, through which there is no current, represents 0. A closed transistor, through which there is a current, represents a 1.

Operations can be achieved by connecting multiple transistors. A transistor can be used to control a second; in fact, it enables or disables the transistor depending on the state of the second transistor. This is called a door because the arrangement can be used to allow or stop a current.

The entries of an ALU are the data to be operated, called operands, and a code that indicates the operation to be performed; the output of the ALU is the result of the operation performed. In many designs, the ALU also has state inputs or outputs, or both, that transmit information about a previous operation or a current operation, respectively, between the ALU and the status registers External.

An ALU is a combinational logic circuit, which means that its outputs will change asynchronously in response to input changes. In normal operation, stable signals are applied to all ALU inputs and when enough time is passed (called "propagation delay") for the signals to propagate through the ALUs, the result of the ALU operation appears. in the ALU the exits. The external circuits connected to the ALU are responsible for ensuring the stability of the ALU's input signals throughout the operation and for allowing sufficient time for the signals to propagate through the ALU beforehand. Shows the result of the ALU.

In general, external circuits control an ALU by applying signals to its inputs. Typically, the external circuits use sequential logic to control the operation of the ALU, which is reinforced by a clock signal of a sufficiently low frequency to guarantee sufficient time for the ALU outputs to stabilize under the conditions of the most worst case also.

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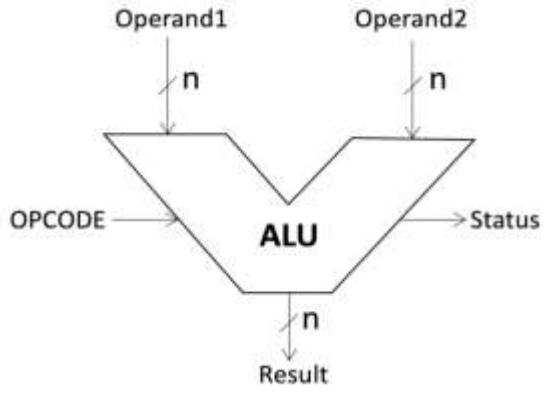

Figure 1 : Basic ALU Design

ALU is getting smaller and more complex nowadays to allow the development of a more powerful system but a smaller computer. However, some limiting factors slow down the development of IC chip more complex and are IC manufacturing technology, designer productivity and design costs. The growing demand for large scale high speed integration (VLSI) can be addressed at different levels of design, like the architecture, the circuit, the design and the level of process technology. At the level of the design of the circuit, there is considerable potential for speed improvement through the appropriate choice of a logical style for implementation combinatorial circuits. This is because all the important parameters that govern the speed switching capability, Transition activity and short-circuit currents are strongly influenced by the chosen logical style. That depends on application, the type of circuit to be implemented and the design technique used, different aspects of the performance be important In the past, such parameters as low power dissipation, small area and low cost issues of concern, while speed considerations attract the attention of the scientific community associated with the VLSI design.

II. DESIGN OF 8 BIT ALU

This ALU operate on 8 bit input. It performs arethematic and logical operations. This gives appropriate output. 8 bit ALU performs 8 operations. There are 2 data inputs and one select line. According to select line input appropriate operation is performed between 2 inputs. Output of this 8 bit ALU is connected between ROM and RAM. A number of basic arethematic and bitwise logic functions are performed in the ALU. ALU can be used in complex operations, system processing and execution of any program.

TABLE1: BASIC OPERATION OF 8BIT ALU DESIGN

S.no.	Input value of S	Operation
1	000	A + B
2	001	A – B
3	010	A + 1
4	011	A - 1
5	100	A | B
6	101	A & B
7	110	A ^ B
8	111	~A

A. VERILOG PROGRAMME OF 8BIT ALU

```
Module ALU (a, b, s, yout, cf);

input [3:0] a;
wire [3:0] a;
input [3:0] b;
wire [3:0] b;
input [2:0] s;
wire [2:0] s;
output [3:0] yout;
reg [3:0] yout;
output cf;
reg cf;
reg [4:0] temp;

always @ ( a,b,s )
 begin
    if ( s  == 3'b000)
      begin
            temp = {0,a} + {0,b};
            yout = temp [3:0];
            cf = temp [4];
```

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```
    end
  else if ( s == 3'b001)
    begin
          temp = {0,a} - {0,b};
          yout = temp [3:0];
          cf = temp [4];
    end
  else if ( s == 3'b010)
    begin
          temp = {0,a} +5'b00001;
          yout = temp [3:0];
          cf = temp [4];
    end
  else if ( s == 3'b011)
    begin
          temp = {0,a} -  5'b00001;
          yout = temp [3:0];
          cf = temp [4];
    end
  else if ( s == 3'b100)
    begin
          temp = a | b;
          yout = temp [3:0];
          cf = temp [4];
    end
  else if ( s == 3'b101)
    begin
          temp = a  & b;
          yout = temp [3:0];
          cf = temp [4];
    end
  else if ( s == 3'b110)
    begin
          temp = a ^ b;
          yout = temp [3:0];
          cf = temp [4];
    end
  else if (s == 3'b100)
    begin
          temp = ~a;
          yout = temp [3:0];
          cf = temp [4];
    end
  end
endmodule
```

B. RTL VIEW OF 8BIT ALU

In the design of digital circuits, the Record Transfer Level (RTL) is a design abstraction that models a synchronous digital circuit in terms of digital signal (data) flows between hardware registers and the logical operations performed on these signals. .

The abstraction at the transfer log level is used in hardware description (HDL) languages such as Verilog and VHDL to create high-level representations of a circuit, from which the lower-level representations and, finally, the actual wiring It can be derived. The RTL level design is a typical practice of modern digital design.

Designers use a description of the Design Log Transfer Level (RTL) to perform optimizations and offsets early in the design flow. The presence of functional blocks in a description of RTL makes the complexity of the architectural design much more manageable, even for larger chips, because RTL has a sufficiently greater granularity than the level descriptions of the gate or circuit.

The Basic RTL View of the proposed 8Bit ALU is shown in the figure 2 which is gives the basic implementation design idea about the proposed 8 bit ALU design regarding its inputs and outputs in the form of the block diagram.

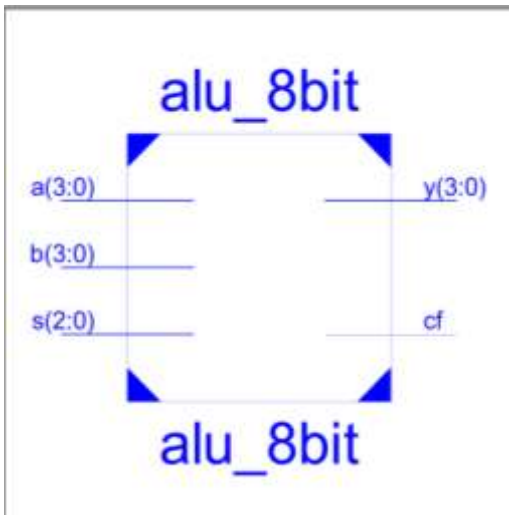

Figure 2 : BASIC BLOCK DIAGRAM OF 8Bit ALU.

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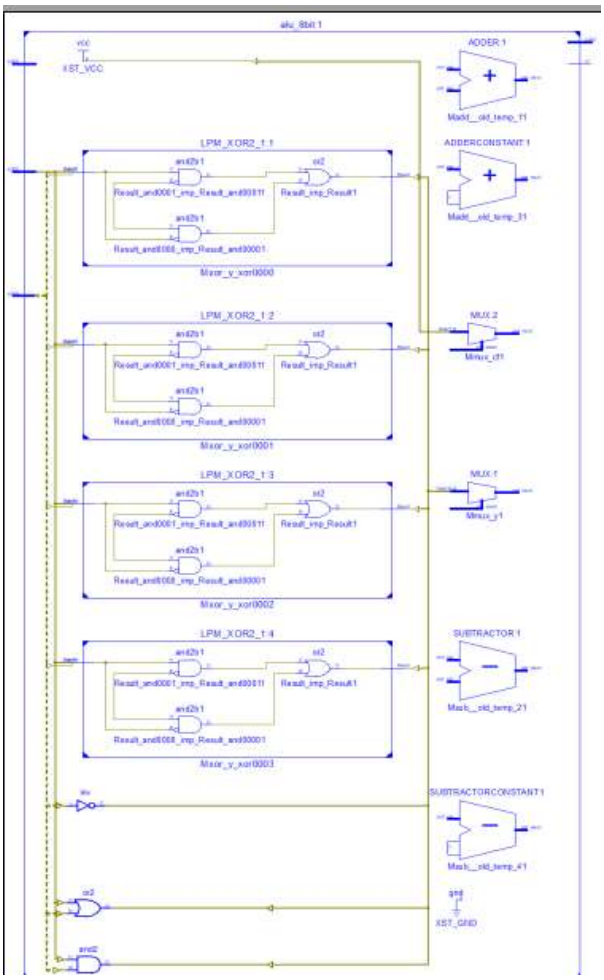

Figure 3 : Logical Design of 8Bit Proposed ALU

C. SIMULATION OF 8 BIT PROPOSED ALU

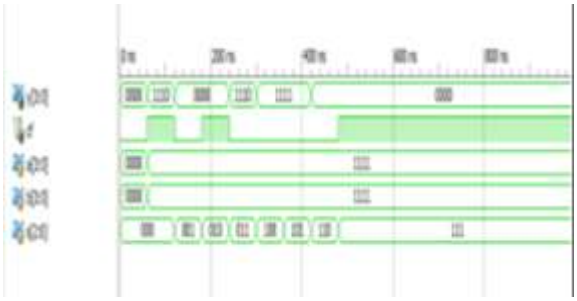

Figure 4 : Output waveform of 8 bit ALU

III. DESIGN OF 16 BIT ALU

This ALU operate on 16 bit input. It performs arethematic and logical operations. This gives appropriate output. 16 bit ALU performs 16 operations. There are 2 data inputs and one select line. According to select line input appropriate operation is performed between 2 inputs. Output of this 16 bit ALU is connected between ROM and RAM. A number of basic arethematic and bitwise logic functions are performed in the ALU. ALU can be used in complex operations, system processing and execution of any program.

TABLE2: BASIC OPERATION OF 16 BIT ALU DESIGN

S.no	Input value of S	Operation
1	0000	A + B
2	0001	A – B
3	0010	A * B
4	0011	B – A
5	0100	A + 1
6	0101	A - 1
7	0110	A + B + 1
8	0111	A - B – 1
9	1000	A | B
10	1001	A & B
11	1010	A ^ B
12	1011	~A
13	1100	~B
14	1101	~(A | B)
15	1110	~(A & B)
16	1111	(A & B) + 1

We executed the Verilog code for the designing of 16bit ALU. The RTL view of the proposed 16 bit ALU is shown in the figure 5 and the logical design implementation of the proposed 16 Bit alu is shown in the figure 6. The output waveform of the 16Bit ALU is shown in the figure 7.

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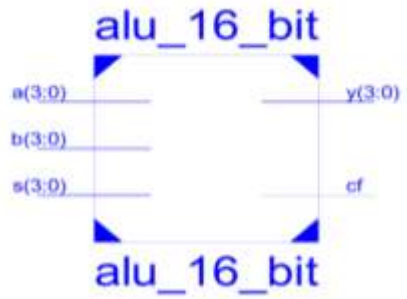

Figure 5: BASIC BLOCK DIAGRAM OF 16 BIT ALU

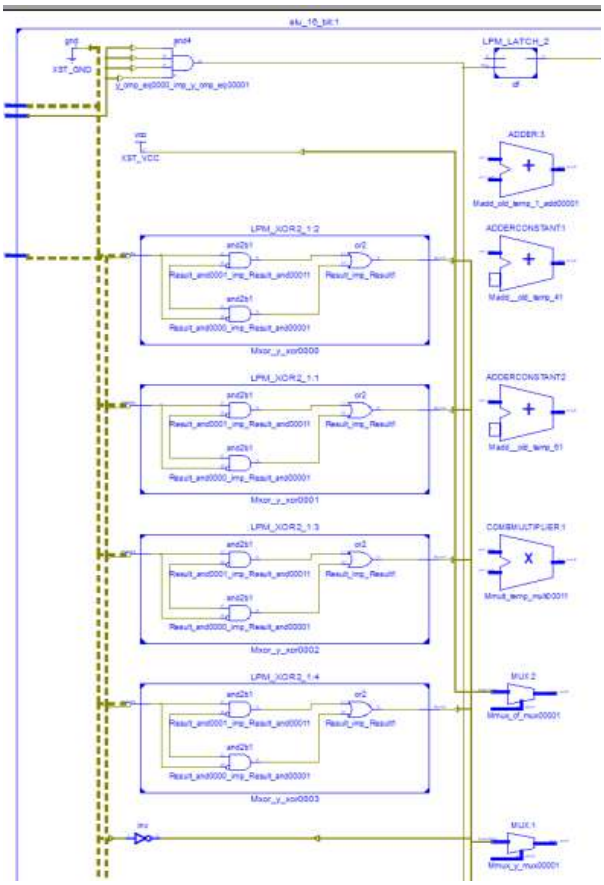

Figure 6 : LOGICAL DESIGN OF 16 BIT ALU

A. SIMULATION OF 8 BIT PROPOSED ALU

Figure 7 : OUTPUT WAVEFORM OF 16 BIT ALU

IV. CONCLUSION

This article presented a new idea to design ALU 16 bits of a processor. It was implemented in the SPARTAN-3E FPGA device. FPGA design offers greater design flexibility. The design is compact and scalable without any change of material. Here, the synthesis tool optimizes the FPGA design architecture for ALU. As a result, additional features can be added to the existing design without any change in Equipment.

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