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DESIGN OF OPERATIONAL TRANSCONDUCTANCE AMPLIFIER FOR APPLICATION IN ACTIVE FILTERS: A REVIEW

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Abstract— **Operational Transconductance Amplifier (OTA) is an amplifier that takes differential voltages as an input and produces current as an output. The OTAs are the significant structure for the design of analog circuits which were prior implemented by utilizing Op amps. This paper shows a review on various procedures for the structure of OTA and further execution of active filters utilizing the proposed OTA. This paper assists the future analysts to develop better OTA in the matter of low power utilization, high frequency operation and linearity.**

Keywords— **Operational Transconductance Amplifier (OTA), Low power, Topologies, Active Filters.**

I. INTRODUCTION

Due to the growing advancement in the architecture of analog designs, the requirement for more and more compact devices with lower energy consumption has been raised. The demand for small gadgets and System-On Chip (SOC) have been constraining the designers to build up the small circuits with low voltage and less power dissipation. Low voltage and low power IC design have been given much attention because power consumption is an essential characteristic in VLSI circuits. The reduction in power consumption and supply voltage helps in achieving higher operating speeds (Rodrigues & Sushma, 2019). However, reducing the supply voltage affects various performance parameters. Therefore, new strategies are required to obtain the appropriate linearity, bandwidth and gain (Gaonkar, Sushma, & Fathima, Design of high CMRR two stage Gate Driven OTA using 0.18 µm CMOS Technology, 2016). The design and execution of such circuits is very difficult task for the circuit originators (Rodrigues & Sushma, 2019).

The growing requirements for low power consumption as well as low power supply circuits arises the significance of operational transconductance amplifiers in analog systems (Tahseen & Singh, 2017). Earlier Op amps were used for the implementation of analog circuits. But because of its frequency limit characteristics, more power consumption and low output impedance, OTAs are preferred over Op amps (Gaonkar, Sushma, & Fathima, Design of high CMRR two stage Gate Driven OTA using 0.18 µm CMOS Technology, 2016). For several analog systems, OTA is one of the significant structure blocks. These provide simplicity in design, faster operation as compared to conventional Op amp structures along with minimum component count (Geiger & Sanchez-Sinencio, 1985). Several topologies such as Series parallel Gate driven technique (Rodrigues & Sushma, 2019), Source degeneration technique (Garradhi, Hassen, & Besbes, 2016), Bulk driven technique (Sushma, Gaonkar, Gurumurthy, & Fathima, 2016), Current division technique (Rakus, Stopjakova, & Arbet, 2012) can be used for designing OTA. The simulation results of these techniques are shown in the literature.

The paper is outlined into 7 Sections. Following the Introduction, the paper explains the Operational Transconductance Amplifier (OTA) and Bi-quad Gm-C Filter in Section II. Section III explains various topologies of OTA. Section IV deals with the overview of some previous works. Section V describes the limitations & design challenges of the existing system. Section VI focuses on future scope. Section VII explains the conclusion.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BI-QUAD GM-C FILTER

An amplifier that accepts differential voltages as an input and provides output in the form of current. Therefore, referred to as a voltage-controlled current source. The symbol of OTA is shown in Figure 1.

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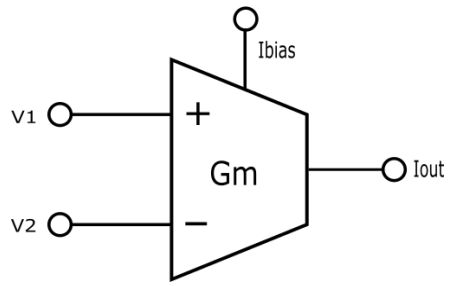

Figure 1: OTA Symbol

V_1 and V_2 are the non-inverting and inverting input voltages. Bias current is used to control the amplifier gain and this current is relative to the transconductance of OTA (Rodrigues & Sushma, 2019). The two-stage block diagram of OTA is shown in Figure 2.

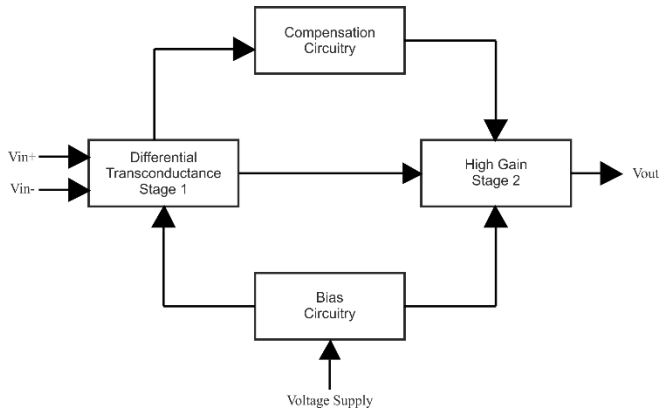

Figure 2: Block Diagram

The diagram includes a differential transconductance stage which produces the input of an operational amplifier which is trailed by a common source second stage. The subsequent stage improves the DC gain and expands the yield voltage swing with respect to the given supply voltage. In order to establish the operating point for each transistor, bias circuitry is used. The compensation circuitry is used to achieve stability (Gaonkar & Sushma, Modeling, Design and Analysis of High CMRR two stage Gate Driven Operational Transconductance Amplifier using 0.18 µm CMOS Technology, 2016).

The OTA finds applications in filters, compact devices, sensors, bio-medical signal amplification and analog to digital converters (Gaonkar, Sushma, & Fathima, Design of high CMRR two stage Gate Driven OTA using 0.18 µm CMOS Technology, 2016). There are various circuit structures for the implementation of Active filters in CMOS such as OTA-C structure (Kumngern & Dejhan, 2009), Gm-C structure (Garradhi, Hassen, & Besbes, 2016) (Sushma, Gaonkar, Gurumurthy, & Fathima, 2016), Op-amp RC structure, and Switched capacitor structure (Rakus, Stopjakova, & Arbet, 2012) etc. Out of these structures, Gm-C is favored as it offers a simple arrangement with minimized power consumption & less area. Gm-C filters depend on voltage to current converters or transconductance and capacitance in order to obtain the transfer function of the filter (Rodrigues & Sushma, 2019). The design of Bi-quad Gm-C filter is shown in Figure 3.

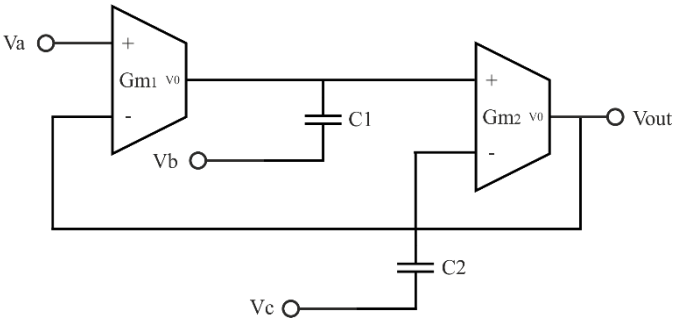

Figure 3: Bi-quad Gm-C Filter

By choosing the suitable inputs, this circuit can be arranged to low pass, band pass and high pass filter (Rodrigues & Sushma, 2019).

Input conditions:

1) **Low pass filter** Va= Vin, where Vb and Vc are connected to ground.

2) **Band pass filter** Vb= Vin, where Va and Vc are connected to ground.

3) **High pass filter** Vc= Vin, where Va and Vb are connected to ground *(Sushma, Gaonkar, Gurumurthy, & Fathima, 2016).*

III. Various OTA Topologies

Depending upon its operation, OTAs are classified into four categories.

A. Single-stage OTA-

The circuit of Single stage OTA is shown below in Figure 4.

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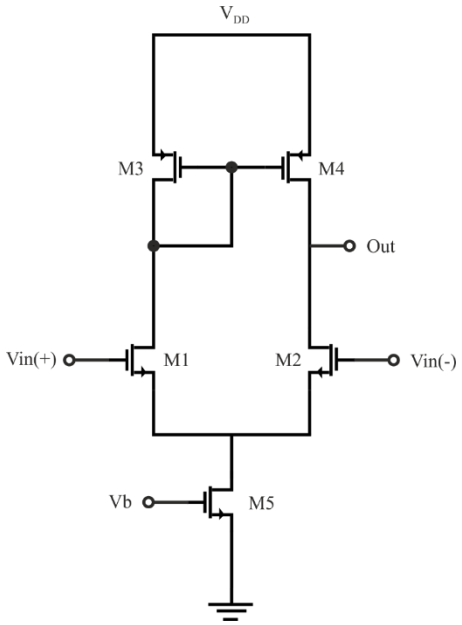

Figure 4: Single-stage OTA

It consists of a differential input pair (M1 and M2) and a current mirror source (M3 and M4). MOSFET M5 is involved in biasing activity (Vadodaria, Patel, & Popat, 2014).

Pros: Simple, fast and low power consumption
Cons: Low gain

B. Two-stage OTA-

The design of two-stage OTA is displayed in Figure 5.

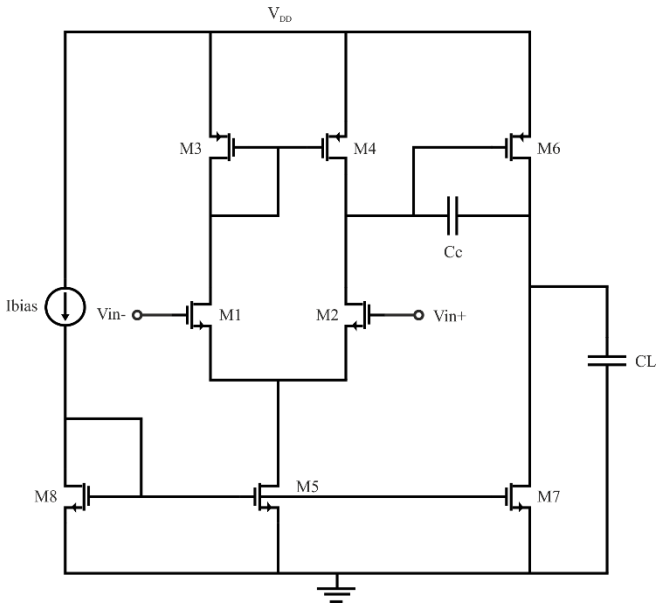

Figure 5: Two-stage OTA

This two-stage design is similar to that of the single stage. In this design, MOSFETs M1and M2 forms a differential pair and MOSFETs M3 and M4 forms a current mirror. M6 and M7 MOSFETs are considered as the second stage. This stage is added for the improvement of gain. M5 and M8 are used to perform biasing activity A coupling capacitor Cc is used to couple the two stages (Rani & Dhanoa, 2017).

Pros: High gain, Highest Output swing
Cons: Slow

C. Telescopic Cascode OTA-

The configuration of Telescopic Cascode OTA is shown in Figure 6.

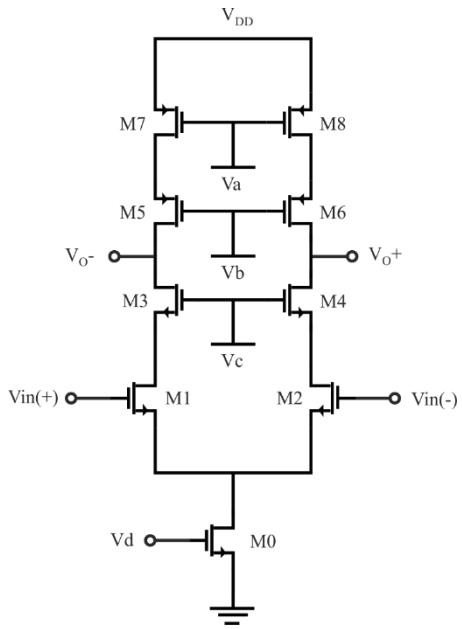

Figure 6: Telescopic Cascode OTA

Due to the low output impedance of single stage OTA, it exhibits low amount of gain. Therefore, some MOSFETs are added at the output in order to increase the output impedance. These MOSFETs are placed on each other and thereby helps in improving the gain. This configuration is known as Cascode (Pandya & Shah, 2013).

Pros: Fastest and low power consumption
Cons: Moderate output swing

D. Folded Cascode OTA-

The circuit diagram of Folded Cascode OTA is presented in Figure 7.

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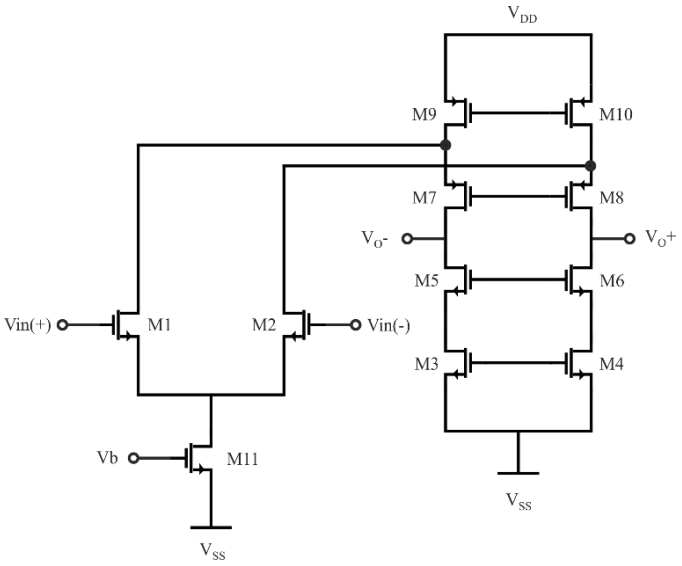

Figure 7: Folded Cascode OTA

The first stage comprises of four MOSFETs at the output side and a differential NMOS input pair. The second stage is in cascade with the first in order to obtain high gain.

Pros: Fast, Moderate power consumption
Cons:

1. This OTA is having two extra legs which will in turn increases the power dissipation.
2. Having more devices, this OTA contributes in adding thermal noise to the signal (Pandya & Shah, 2013).

A comparison of different OTA topologies is described in Table I (Razavi, 2000).

Table I: Comparison of Topologies

Topology	Speed	Gain	Power Consumption	Output Swing
Single stage	Fast	Low	Low	Low
Two stage	Slow	High	Moderate	Highest
Telescopic Cascode	Fastest	Moderate	Low	Moderate
Folded Cascode	Fast	Moderate	Moderate	Moderate

IV. Literature Review

This chapter contains some of the previous work that has been already done in analog design. It includes the techniques that have been used for modelling of OTA and various approaches for the implementation of filters using OTA.

S.N. Rodrigues et al. (Rodrigues & Sushma, 2019) have proposed the design of high gain low transconductance OTA utilizing series-parallel gate driven technique. The second-order Bi-quad Gm-C low pass and high pass filters are then realized by using the proposed OTA.

S. Gaonkar et al. (Gaonkar, Sushma, & Fathima, Design of high CMRR two stage Gate Driven OTA using 0.18 µm CMOS Technology, 2016) have proposed a gate driven approach for designing a two-stage Operational Transconductance Amplifier (OTA) having high CMRR. The design is implemented in 180 nm CMOS process technology using the Cadence Virtuoso tool.

S.J. Tahseen et al. (Tahseen & Singh, 2017) have realized a different OTA by employing bulk driven and pseudo-differential technique.

R. L. Geiger et al. (Geiger & Sanchez-Sinencio, 1985) have discussed the applications of OTAs in filters, impedances, and voltage-controlled amplifiers.

K. Garradhi et al. (Garradhi, Hassen, & Besbes, 2016) have introduced another methodology for planning low power and low voltage OTA utilizing the source-degeneration technique. The proposed OTA provides a wide transconductance adjustment range, large differential input voltage capability and decreased power utilization of 1.2µW. The OTA is then used to execute the Gm-C filter.

P.S. Sushma et al. (Sushma, Gaonkar, Gurumurthy, & Fathima, 2016) have described a concept to design an OTA using bulk driven design technique. The proposed OTA is useful for ultra-low power, low voltage bio-medical applications as the voltage provided to OTA is very low 0.4 V. The proposed OTA is then used to structure Bi-quad & Gm-C filters.

M. Rakus et al. (Rakus, Stopjakova, & Arbet, 2012) have presented the various topologies of Bulk driven and Gate driven current mirrors that are planned in 90 nm CMOS process innovation. A correlation of gate driven and bulk driven topologies is shown.

S. Gaonkar et al. (Gaonkar & Sushma, Modeling, Design and Analysis of High CMRR two stage Gate Driven Operational Transconductance Amplifier using 0.18 µm CMOS Technology, 2016) have proposed a strategy for modeling, structure, and interpretation of a two-stage gate driven OTA having high CMRR. No extra voltage source is required for biasing, subsequently diminishing the expense & also less power is consumed, which can be further used for signal processing in bio-medical applications.

M. Kumngern et al. (Kumngern & Dejhan, 2009) have proposed a concept of a voltage-mode universal bi-quadratic filter having a single input and three outputs utilizing four basic CMOS OTAs & two grounded capacitors. The low-pass, high-pass and band-pass filters are realized by using the proposed Bi-quadratic filter without the condition of component matching.

J.Pérez-Bailón et al. (Perez-Bailon, Marquez, Calvo, Medrano, & Sanz-Pascual, 2018) have discussed a concept of first-order Gm-C LPF having tunable cut-off frequency lying in the range

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250 MHz-14 kHz for a temperature span ranging between -40ºC to 120ºC. The proposed low pass filter, in comparison with the previous work produces an enhancement in dynamic range, while preserving compact size and low power consumption.

H. S. Raghav et al. (Raghav, Singh, & Maheshwari, 2013) have designed a low voltage operational transconductance amplifier that can be used for bio-medical purposes. The proposed OTA's performance meets all the requirements for its realization in Bio-medical compact devices.

A. Yodtean et al (Yodtean, 2014) has proposed a method for the design of CMOS OTA that leads to attaining a wide linear input range & at the same time maintains high performance. The proposed OTA is then used to execute the Gm-C Bi-quad filter. The simulation is carried out in the spectre simulator by using 180 nm CMOS technology.

Dr. R.S Mathad et al (Mathad, 2014) has explained a method to design a low-frequency filter by using OTA. Simplicity in design is observed on comparison with structures based on the op-amp. All the specifications such as portability, low supply voltage & low component are obtained.

Various techniques used are shown in Table II.

Table II: Survey of different Parameters of OTA

Ref.	Tech.	Parameters				
		V_{DD} (V)	CMRR (dB)	Phase Margin	Gain (db)	Power Consumption
(Mythry, Reddy, Riyazuddin, Snehitha, & Shamili, 2015)	180 nm	3.0	----	171.0º	182.9	----
(Gaonkar, Sushma, & Fathima, Design of high CMRR two stage Gate Driven OTA using 0.18 µm CMOS Technology, 2016)	0.18 µm	2.5	96.0	75.0º	46.5	----
(Rodrigues & Sushma, 2019)	180 nm	1.6	63.0	62.6 º	21.2	194.3 nW
(Gaonkar & Sushma, Modeling, Design and Analysis of High CMRR two stage Gate Driven Operational Transconductance Amplifier using 0.18 µm CMOS Technology, 2016)	0.18 µm	1.6	70.0	76.0º	34.1	----
(Raghav, Singh, & Maheshwari, 2013)	180 nm	1.0	104.9	----	67.8	7.2 µW
(Perez-Bailon, Marquez, Calvo, Medrano, & Sanz-Pascual, 2018)	0.18 µm	1.0	----	----	----	1.8 µW
(Garradhi, Hassen, & Besbes, 2016)	0.18 µm	0.9	151.0	----	61.9	1.2 µW
(Jusoh W. , Ruslan, Ahmad, Jubadi, & Sanudin, 2019)	90 nm	0.9	140	----	55.9	9.38 µW
(Yodtean, 2014)	0.18 µm	0.8	148.0	86.0º	76.0	4.6 µW
(Jusoh & Ruslan, Design of Low-Power Bulk-Driven Balanced OTA in 90nm CMOS Technology, 2018)	90 nm	0.5	51.5	----	29.6	4.3 µW
(Jusoh & Ruslan, Design and analysis of current mirror OTA in 45 nm and 90nm CMOS technology for bio-medical application, 2020)	90 nm	0.5	102.6	----	45.3	28.42 nW
	45 nm	0.5	93.2		45	28.2 nW
(Sushma, Gaonkar, Gurumurthy, & Fathima, 2016)	180 nm	0.4	82.0	57.0º	----	281.5 nW

The various filter parameters studied in this review are shown in Table III.

Table III: Survey of Filter Parameters

Structure Used	Tech.	Supply Voltage (V)	Cut-off Frequency	
			LPF	HPF
Bi-quad Gm-C (Gaonkar & Sushma, Modeling, Design and Analysis of High CMRR two stage Gate Driven Operational Transconductance Amplifier using 0.18 µm CMOS Technology, 2016)	0.18 µm	2.5	488.0 Hz	46.0 KHz

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OTA-C (Mathad, 2014)	----	1.8	3.1 mHz Using Single OTA	1.5 mHz Using two OTAs	----
Bi-quad Gm-C (Rodrigues & Sushma, 2019)	180 nm	1.6	586.0 Hz		380.0 Hz
Gm-C (Garradhi, Hassen, & Besbes, 2016)	0.18 µm	0.9	750.0 KHz		760.0 KHz
Gm-C (R, Taralkar, M.H., & Y.B., 2017)	180 nm	0.5	250.0 Hz		----
Bi-quad Gm-C (Sushma, Gaonkar, Gurumurthy, & Fathima, 2016)	180 nm	0.4	47.3 Hz		373.7 Hz

From the above literature review, it may be concluded that for designing the operational transconductance amplifier, a series-parallel gate driven technique gives superior outcomes regarding linearity, power, and transconductance. Likewise, for the usage of Active filters utilizing OTA Gm-C structure is favoured as it offers a simple arrangement with minimized power consumption & less area (Rodrigues & Sushma, 2019).

V. OTA Design Challenges and Limitations

Due to the continuous decrease in the component size of the transistor, power consumption & supply voltage to obtain the higher operating speeds, results in a decrement in the linearity of the analog circuits and shrinkage of dynamic range. The enhancement of the dynamic range is a major challenge in the low voltage OTA design. Likewise, the decrease in supply voltage degrades the circuit execution in the matter of voltage swing and accessible transfer speed. The performance loss is reduced by reducing threshold voltage (Vth) of MOSFETs to some level but in turn, an increase in power dissipation is noticed (Sheikh, Dahigaonkar, & Lohana, 2012). Another challenge that requires to be addressed for low power low voltage applications is reduced power consumption (Poddar & Ali, 2015).

Moreover, while designing the filter based on OTA, most of the existing work approaches the problem either by altering the already existing op-amp circuits by including some other OTAs and passive components or by making filter properties self-dependent and free from transconductance gain by applying feedback. In each case, circuits were complicated to tune and usually component intense (Geiger & Sanchez-Sinencio, 1985).

VI. Future Scope

The maximum frequency up to 40GHz for the CMOS 0.18-µm technology has been widely used in industrial applications all over the world. As the world moves into the nano age in the 21st century, it was a need of time to make the compact design of OTAs too and in the mean-time, a much higher frequency than 40 GHz is feasible for further research in the CMOS 130-nm, 90-nm, 65-nm, and 45-nm advancements. The three main matters of the subject to make the CMOS OTAs applications more reliable are high frequency, high linearity, and low power (Sheikh, Dahigaonkar, & Lohana, 2012).

A lot of research is under the pavement for implementing the new CMOS OTAs design with the higher frequency which will be utilized as a fundamental design for a few applications such as microwave and RF. Not only higher frequency but also the OTAs design for high linearity, less power, and lower supply voltage are the topic for further research for the researchers in this field so that these OTAs semiconductor technologies can be widely used in the commercial industry (Sheikh, Dahigaonkar, & Lohana, 2012).

VII. Conclusion

OTA being the significant building block for various analog circuits also finds suitable applications in the RF and microwave industry. There are several techniques which can be used to optimize the suitable design of CMOS OTAs such as linearity and power optimization for various industrial application. But these techniques need to be used carefully as each of them has some positive and negative impact on the design (Poddar & Ali, 2015).

For obtaining the lower power consumption and increased bandwidth of OTAs, the choice of topology plays a significant role in designing a circuit. The main aspects to make the CMOS OTAs applications highly efficient for commercial purposes are higher frequency, higher linearity, and lower power. The IC-researchers have to make a cut-off among these factors for designing a better and practical CMOS OTAs designs (Sheikh, Dahigaonkar, & Lohana, 2012). The higher frequency and low voltage aspects are achievable by scaling down the size of the device (Poddar & Ali, 2015).

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