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DESIGN OF DIGITAL DOWN CONVERTER AND SIGNAL DETECTION TECHNIQUES FOR SOFTWARE DEFINED RADIO

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Abstract— **Software Defined Radio (SDR) is the ubiquitous technology employed in Electronic Communication Systems. Widespread availability of multi-processor SoC technologies lead the way to replace the analog hardware blocks with software driven flexible heterogeneous computing blocks. One of the potential requirement of Software defined Radio/Receiver is assessment of spectrum occupancy over the specified frequency spectrum. The SDR has fast analog-to-digital converter (ADC) that digitizes the band limited RF or IF signals followed by Digital Down Converter (DDC) that optimizes the bandwidth (BW) and output data rate. In many applications, the signal of interest represents a small proportion of the input BW. Spectrum occupancy is estimated by converting time domain signals at the output of DDC to frequency domain and applying detection threshold on the spectrum. This is achieved through Fast Fourier Transform (FFT) technique. Active signals within the pass band are detected based on the estimated Noise riding threshold of the spectral data. In this paper, DDC and FFT blocks are designed for implementation on FPGA. Vivado 2018.1 version tool is used in the design and development of the firmware. Broad specifications are RF = 100 to 1000 MHz, Second IF = 75 MHz, instantaneous BW = 40 MHz, ADC sampling rate, f_s = 100 MHz.**

Keywords— **SDR, DDC, FFT, FIR filter, NCO, CIC filter**

I. INTRODUCTION

The Software Defined Radio (SDR) is the ubiquitous technology used in wireless communication systems for exchange of information between source and destination. In this paper, two key functional blocks of Software defined receiver are designed for detecting signals using Spectrum processing concept. Digital down conversion is the process of down sampling the digitized input signals by programmable decimation factor (as per desired information BW) without loss of information. Either of two sampling schemes are used for digitizing signals, viz., direct RF sampling (where RF is lower than ADC sampling rate) or bandpass sampling (where at least one analog frequency down translation is needed) of Intermediate Frequency (IF) Signal. The digitized signals are streamed to the DDC for translating real band pass signal to complex baseband (digital I, Q) output. DDC BW is set by programming decimation factor followed by digital filtering to remove unwanted artefacts of the signal. The digitized input signals to the DDC are real which are multiplied with programmable complex local oscillator outputs generated from numerically controlled oscillator (NCO). The resultant signals are passed through cascaded integrator-comb (CIC) filters for sample rate conversion. The CIC outputs are further processed through a compensating FIR filter to overcome the shortcomings of CIC decimator, namely pass band droop and wide transition region. In the present application, the DDC brings the passband signal centered at IF to baseband and down samples the signal by programmable decimation factor to result output sample rate that commensurate with the desired BW.

FFT based wideband spectrum processing enables detection of all intercepted signals present within the instantaneous BW simultaneously. The Spectrum processing transforms the time-domain complex baseband signal to Frequency-domain. FFT length (K) could be programmed to facilitate different spectral resolutions *($\Delta f = fs/K$)* that could be depicted on the display in frequency domain. Blackman-Harris window function is used for conditioning the data before performing FFT. Window coefficients are loaded a priori in the memory based on the FFT length, which are used before initiating FFT process.

II. OBJECTIVES AND MOTIVATION

Radio Systems have undergone several generations since World War I, both in terms of hardware architectures and technologies. As electronic and software technologies advanced, the current trend is aimed towards all-digital

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reconfigurable and programmable architectures. An ideal "*Software Defined Radio*" operates only with digital components, where ADC/DAC is directly connected to the Antenna. However, high performance radio systems needs RF/Microwave amplifiers and at least one analog frequency translation before the signals are applied to ADC/DAC. Digital Up-converter (DUC) is associated with transmitter as DDC is associated with the Receiver. DUC is the inverse process of DDC, where complex digital base band signal is up-translated to digital IF which in turn drives DAC to result analog IF output. DDC/DUC simplifies SDR design and brings in great flexibility in terms of programmable IF BW. In this paper, only DDC is considered. As stated the main objective of this paper is detection of signals within a wideband using FFT techniques. Unlike analog techniques, FFT allows processing and detection of all signals present simultaneously within the wider band. Automatic detection is facilitated by estimating the noise floor within the spectrum. DDC and FFT blocks are designed to meet an instantaneous BW of 40 MHz. Since the BW is very high FPGA based hardware realization is envisaged in the design. Implementation of these blocks in FPGA offers an optimal design in terms of size, weight and power (SWaP) consumption. The design also envisages porting of VHDL/Verilog code on any FPGA or FPGA based MP-SoC hardware. Finally the design is adoptable to programmable IF, LO and BWs with minor re-work on the Verilog code.

III. LITERATURE SURVEY

In [1], the DDC is a significant part of baseband processor that translates real digital samples at RF/IF to complex baseband. The decimation filter is one among the fundamental blocks in DDC. Its construction and functioning influence the performance of the SDR. DDC also does decimation, digital filtering functions to eliminate undesired spectral components and improves the signal-to-noise ratio (SNR) of the received information. Down sampler is a fundamental sampling rate-changing device employed to decrease sampling rate of signal by an integer (or rational) factor. Low pass filter (LPF) is employed in each branch of DDC to decrease the signal BW before decreasing the sample rate. The method of reducing the sampling rate of a signal in a signal processing system is named as decimation. The device that changes the sampling rate of the signal is known as decimator or down sampler. Decimation need to be performed in such a way to avoid the aliasing effects. In general, the decimator performs two functions: filtering and down sampling. The overlapping of the original spectrum with continued replica occurs if the signal is not correctly band limited. Hence, the original signal has to be band limited before down sampling. The requirement of efficient decimation filter is increasing rapidly. This high demand has created interest to design or develop efficient decimation filter structure for DDC in Software defined radio (SDR) applications. Several techniques are available for Spectral estimation. FFT based spectral estimation is especially used to estimate the spectrum in an unknown signal environment.

IV. PROPOSED WORK

Digital Down Converter –

DDC technique is used to select the desired spectral part among the spectrum that exists at the output of ADC. In effect, DDC is a digital down sampler which replaces analog down converter. The main benefit of DDC is conversion of digitized signals to base band with selectable BW.

The digital down converter comprises of:

A. Numerically Controlled Oscillator (NCO)
B. Mixer or Multiplier
C. Cascaded Integrator Comb (CIC) filter
D. Compensating FIR (CFIR) filter.

Explanation of each block follows.

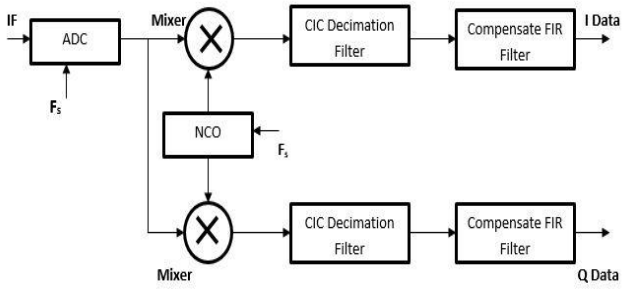

Figure 1. Block diagram of DDC.

A Numerically controlled Oscillator

NCO is a synchronized quadrature digital signal generator that generates sine and cosine signal waveforms with a phase difference of 90°. Several techniques are available for generating the quadrature signals. Here, read-only memory (ROM) look up table method is used. The amplitude values sine and cosine signals are stored in digital format in the ROM. The phase accumulator output acts as address to the ROM to access the corresponding amplitude. As per Nyquist-Shannon's theorem, the number of samples required in each cycle shall be at least two for signal reconstruct without aliasing.

The increment value for the phase accumulator is

$$\theta = F_{clk}/2^N \quad (1)$$

Where θ is the increment value of phase accumulator, F_{clk} is sampling rate of NCO input signal with N-bit width.

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B Mixer

The mixer (or digital multiplier) multiplies digitized input signal fed from ADC with cosine and sine waveform data (generated from NCO) to result in-phase and quadrature outputs, respectively. The mixer output comprises of sum and difference of RF/IF & LO signals including all possible combinations of mixer inputs.

The mixer is characterize by Equation 2 with two different frequencies F1 (RF/IF) and F2 (Local Oscillator / NCO) .

$$Mix(F_1,F2) = (F_1+F_2) + (F_1-F_2) + n(F1 \pm F2) \quad (2)$$

Where n is an integer.

C CIC Filter

The mixer outputs in the DDC need to be filtered to allow desired combination of RF/IF and LO signals and simultaneously eliminate undesired artifacts that result in the mixing process. CIC filter is used in each output branch of DDC to perform this function. A CIC decimation filter [2] does not use multiplier in its implementation and hence economical for its use as first stage filter in the DDC. The CIC filter is a cascade of digital integrators followed by a cascade of combs (digital differentiators) in equal number. Between the integrators and comb filters, there is a digital switch or decimator used to lower the sampling frequency of comb filters with respect to the sampling frequency of the integrators.

An Integrator is a unity feedback coefficient circuit. It works as an accumulator that always runs at higher sampling rate as given in Equation 3.

$$Y[n] = y[n-1] + x[n] \quad (3)$$

Comb filter has delay and subtraction block, which always operates at lower sampling rate Fs/R, where Fs is sampling frequency and R is decimation Factor. Equation 4 represents functionality of Comb circuit.

$$Y[n]=x[n]-x[n-RD] \quad (4)$$

The purpose of decimation filter is to reduce the sampling rate after mixing which is configured between Integrator and Comb circuit. Here, decimation factor is an integer with a power of two [3].

D FIR Filter

Linear phase response is essential in many signal processing applications. While exploiting all the benefits of CIC filter, its phase response need to be compensated using Finite Impulse Response (FIR) filter as shown in Figure 1. FIR filter always follows CIC filter and this combination finally results liner phase response. The decimation factors of CIC and FIR filters are normally higher and lower, respectively for optimum resource utilization. The compensated FIR filter offer linear phase response and always stable. The characteristic equation of FIR filter is given in Equation 5, which is the convolution of input and FIR filter impulse response [4].

$$Y(n) = \sum_{k=0}^{N-1} h(k)\ x(n-k) \quad (5)$$

Where h(k) is impulse response of FIR filter, k=0,1,2……...N-1 and N is the filter length.

Signal Detection Techniques –

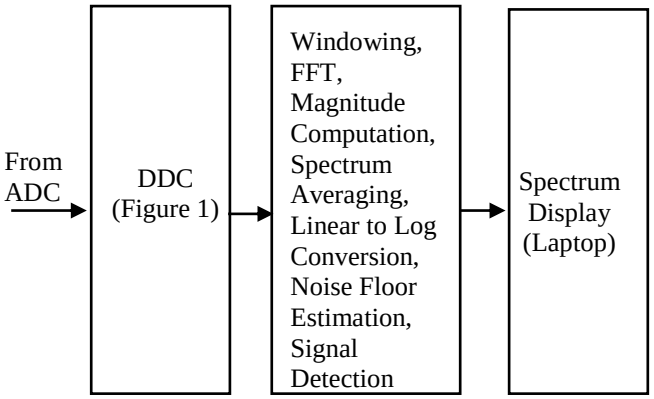

Figure 2. Spectrum Processing

DDC produces complex in-phase (I) and quadrature (Q) data, which are used as input to spectrum processing. FFT is the process of translating time domain data to frequency domain. The spectrum resolution depends on the DDC output sampling rate and FFT length *(Δf = fs/K)*. Before performing FFT, DDC complex IQ data is multiplied with Blackman-Harris window coefficients.

FFT output produces real and imaginary parts of the signals in frequency domain. Multiple FFTs are computed and then averaged to reduce variance and bias of FFT results. The amplitude samples are converted to dBm scale for representation to the external world. Noise floor of the spectrum over the specified frequency range is computed based on median filtering technique. In order to reduce false alarms, SNR margin is added to the noise floor for signal detection. Thus the Noise riding threshold (NRT = Noise Floor + SNR) represents the detection threshold for the signals present in the given frequency range. Typical SNR threshold margin varies (10 to 15 dB).

V. RESULT

The proposed work has been carried out using Xilinx Vivado 2018.2 version, and the results are depicted in Figure

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3. DDC design is simulated for down sampling with selectable decimation factor. Input data rate from ADC to DDC is 100 MHz and output-sampling rate is 50MHz, 25MHz for decimation factor of 2 and 4, respectively. After down sampling and filtering, IQ data undergoes FFT processing and signal detection. The FFT resolution depend on FFT Size. In this case, when the decimation is 2, the output sampling rate would be 50 Mega samples /s and hence the FFT resolution would be, Δf = 50 MSPS/4096 = 12.20703125 kHz.

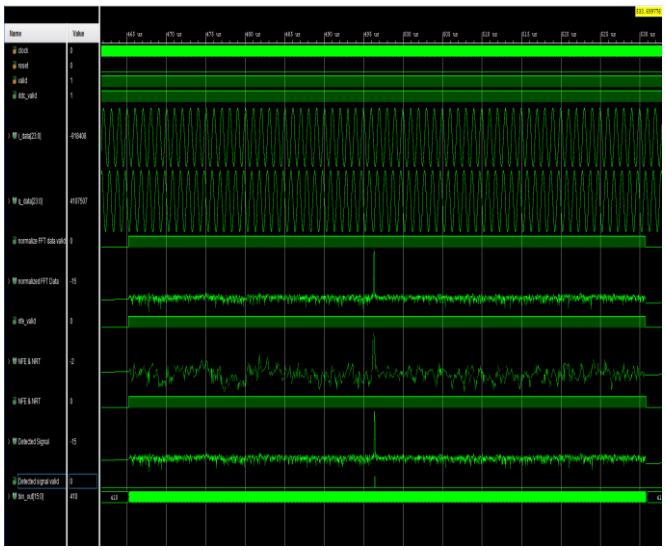

Figure 3. Simulation result in Vivado

The simulated output data carried out in VIVADO have been captured and plotted in MATLAB to verify the simulation result, which is shown in Figure 4. It shows the spectrum processing output, where the signal undergoes windowing, complex FFT computation, spectrum averaging, normalization to 10dBm and conversion to logarithm (dBm) scale. All the simulation work has been carried out under VIVADO development environment. Blue colour represents the active signal, orange colour indicates computed average noise floor and yellow colour indicates NRT (i.e., Noise Floor + SNR Margin). Hence, signals above yellow trace are only detected and reported automatically. SNR margin is a trade-off between false alarms (lower margin) and missed signal detection (higher margin) which could be varied during actual operation.

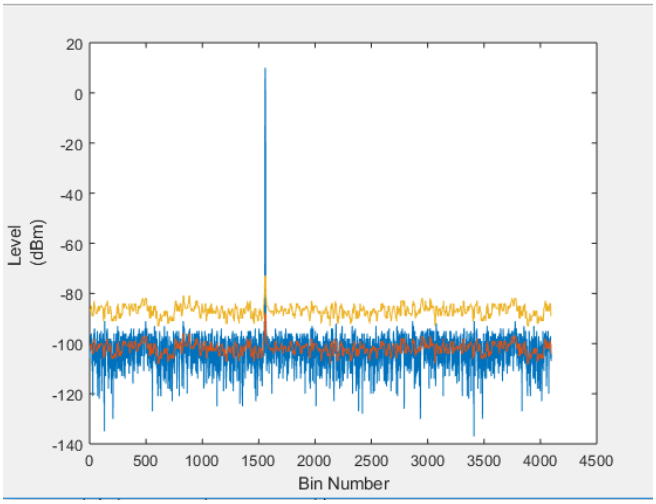

Figure 4. Spectrum processing final output

IV.CONCLUSION

In any modern receiver design for detecting a signal, a DDC and low pass filter are necessary. Designing these blocks are important in advancing technology. Based on result following conclusions are made. CIC and FIR filter are used for down sampling and to remove unwanted signal by selecting cut off frequency. Which are producing Linear Phase response. After DDC, the sample rate is significantly reduced. And signal get detected by FFT and its processing steps.

VI. ACKNOWLEDGEMENT

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