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IMPLEMENTATION OF DECODER USING LDPC CODES ON FPGA

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***Abstract*—Now-a-days the usage of the mobile was increased so the speed of the network should also be increased. So as to improve the speed decoding technique are to be introduced. In 5G technology to increase the throughput and latency LDPC codes and Polar codes are introduced. In this paper we are introducing LDPC codes using Min Sum (MS) algorithm.**

I. INTRODUCTION

Low Density Parity Check (LDPC) codes are a class of linear forward error correcting codes which were first introduced by Gallager in 1963. [8] et al. "Gallager (1962)". The no.of 1's in the parity check matrix are less than no.of 0's then the parity check matrix is referred as low density parity check matrix. If the no.of rows and columns are not equal in the parity check matrix then the matrix is referred as irregular. Similarly if the rows and columns in a parity check matrix are equal then the matrix is referred as regular. In this paper we are considering the irregular parity check matrix for improving the throughput and latency.

Initially LDPC codes are decoded using belief propagation (BP) algorithm but while using the BP algorithm there is complexity in check node computation. By using the Min-Sum algorithm the complexity in the check node computation can be reduced.

In the decoding process there will be a final decision. The final decision is of two types. [5] et al. "Rinu (2015)". Hard decision and Soft decision. Soft decision technique is considered.

Hard Decision: In Hard Decision decoding the receiver 'threshold detector' block receive a stream of bits, where each bit is considered clearly one or zero. As an example received pulses of binary signalling are sampled and the resulting voltages are compared with a single threshold.

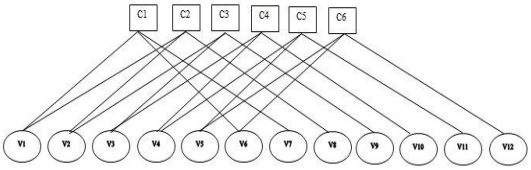
Soft Decision: Hard-decision decoder is majorly operates on data that take on a fixed set of values (0 or 1) such as repetition codes, soft-decision decoder takes input a different range of values. This indicates the dependability of each input data point, and is used to form better estimates of the original data. Therefore, a soft decision decoder than a hard decision decoder. [6] et al. "Fossorier (1995)".

II. LDPC

Low Density Parity Check (LDPC) codes are linear forward error correcting codes that is being used in the 5G communication system. There are two ways to represent a parity check matrix they are mathematical form and graphical form. Mathematical representation uses matrix form whereas Graphical representation uses Bipartite graph. Consider a parity check matrix which consists of less no.of 1's, [7] et al. "MacKay (1999)".

H=

V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	
1	0	0	0	0	1	1	0	0	0	0	0	C1
1	1	0	0	0	0	0	1	0	0	0	0	C2
0	1	1	0	0	0	0	0	1	0	0	0	C3
0	0	1	1	0	0	0	0	0	1	0	0	C4
0	0	0	1	1	0	0	0	0	0	1	0	C5
0	0	0	0	1	1	0	0	0	0	0	1	C6



The rows in the parity check matrix are referred as variable nodes whereas the columns in the parity check matrix are referred as check nodes. [9] et al. "Chutima (2009)". The following graph represents the Bipartite graph for the above parity check matrix,

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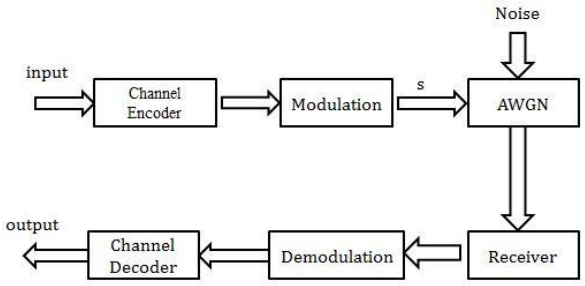
The above bipartite graph represents the parity check matrix which consists of n rows and k columns. The nodes c1, c2, c3, c4, c5, c6 are the check nodes represents the rows and the nodes v1, v2, v3… v11, v12 are the variable nodes that represents the columns in a parity check matrix (H-matrix).

III. BLOCK DIAGRAM

The input to the channel is an analog input. The analog input is then given to the source encoder which converts the analog input to digital, and then the digital input (bit stream) is given as input to the channel encoder. A generator matrix is generated in the encoder and its inverse will be the parity check matrix. By multiplying the parity check matrix and generator matrix we get a codeword consists of 1*n matrix. [6] In the channel encoder the parity bits were added to the information bits. The parity bits, p=n-k; where n is the code length and k represents the information bits. The output of the encoder is nothing but a codeword. The codeword is given to the modulator which performs the bit to symbol operation. [10] et al. "Cheng Kun (2019)", [11] et al. "Porcello (2014)". The modulator we are considering is digital modulation because most of the cell tower uses this modulation technique. The below figure shows the block diagram of the communication channel,

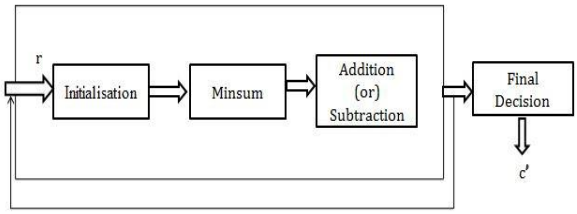


The bits are converted into analog form and transmitted towards the channel. In the channel an Additive White Gaussian Noise is added. The receiver then receives the analog signal which contains some noise over the channel. The layer decoding operations is then performed for the received bits and converts the symbols to bit. Finally the output will be in the analog form by using the source decoder.

IV. MINSUM DECODER

Low Density Parity Check matrix can be decoded using Min-Sum algorithm or Belief Propagation algorithm. [3] et al. "Kumara (2016)", [4] et al. "Jinghu (2005)". In the Min-Sum algorithm there are majorly four steps. They are

1) Initialisation
2) Min-Sum
3) Basic mathematical operation
4) Final decision



In the decoding section the received bits from the channel are in the form of probabilities of the transmitted symbol bits. In the initialisation step the received bits are replaced in the parity check matrix. The received bits are replaced only in the place of 1's in the H-matrix. After the initialisation step, min-sum operation should be performed. Min-sum is performed based on check node. Firstly we have to consider two min values without considering the sign. Check the parity sign for each row. Replace the values of min 1 and min 2 and replace the other values in the row with min 1 value. The addition and subtraction operation will be performed based on the operation required. After all the operations the final decision is performed. In the final decision we consider the threshold values. If the final values are greater than the threshold value then the value is represented as 0, and when the final value is greater than the threshold value then the value is represented as 1. [2] et al. "Kidambi (2009)".

V. IMPLEMENTATION

The MinSum (MS) decoder is designed in the following process,

Step 1: Initialising the received values into the parity check matrix, where 1's are present.

Step 2: Divide the parity check matrix into two layers, consider half of the matrix as layer1 and the other half as layer 2.

Step 3: Firstly consider the layer 1, row 1. In row1 consider the first two min values without considering the signs and then replace the min 1 value with min 2 value and the remaining values in the row with min 1.Now by doing the parity check denote the signs for each column in a row.

Step 4: Add layer 1 values with received values and consider it as sum_1. Replace the sum1 values in layer 2.

Step 5: Consider the min values and replace the first min value with the other and the remaining values in a row with first min value and denote the sign for each column in a row after considering the parities.

Step 6: Now add the layer 2 values with the sum_1 values note it as sum_2 values.

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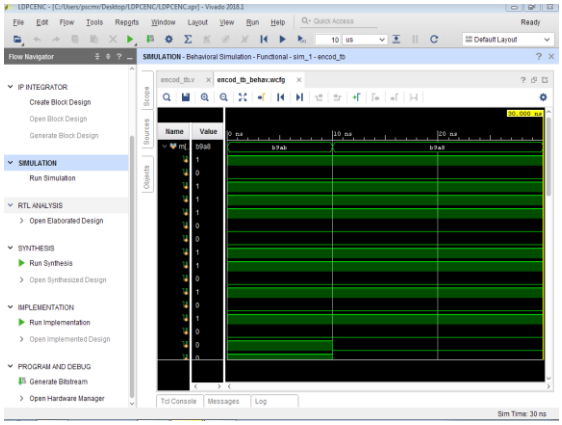
Step 7: Now subtract the layer 2 values with sum_2 values and note it as sum_3.
Step 8: Now initialise the sum_3 values in layer 1 and do the min sum operation as in step 5.
Step 9: Add layer 1 values with sum_3 values and note it as sum_4.
Step 10: Now subtract sum_4 values with layer 2 values and note it as sum_5. Replace the sum_5 values in layer 2
Step 11: Now initialise the sum_5 values in layer 2 and do the min sum operation as in step 5.
Step 12: Add sum_5 values with layer 2 values and note it as sum_6.
Step 13: The last step in this decoding process is the final decision. In this step we are considering the threshold value. The threshold value should be compared with each and every element in sum_6. If the elements in sum_6 are greater than threshold value then the decision will be '0' and if the values are less than threshold value then the decision will be '1'.
These are the steps to be performed in MinSum decoding to achieve high throughput and latency. By using layer decoding techniques the computational complexities are also reduced. [1] et al. "Alami (2011)", [12] et al. "Zarkeshvari (2002)".
Note: The operations are performed only for the values except zero.

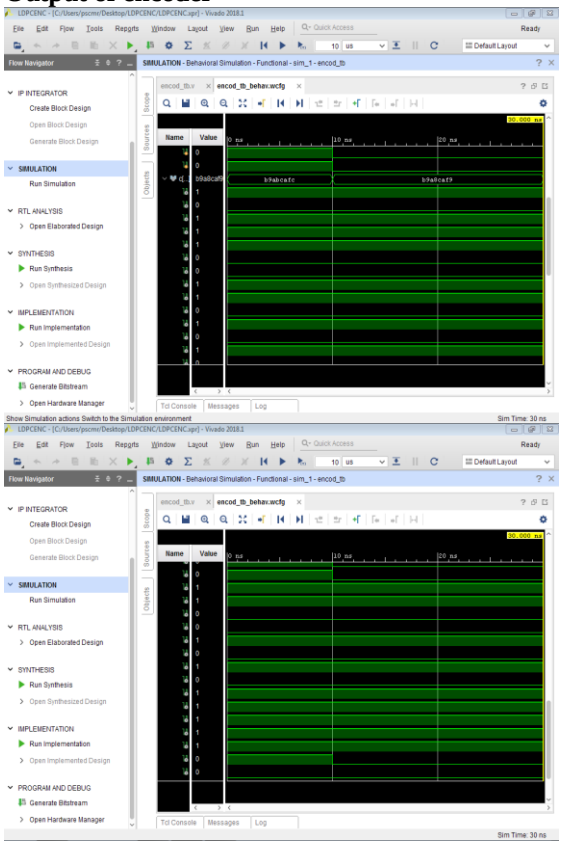
VI. RESULTS AND CONCLUSION

Input message bits



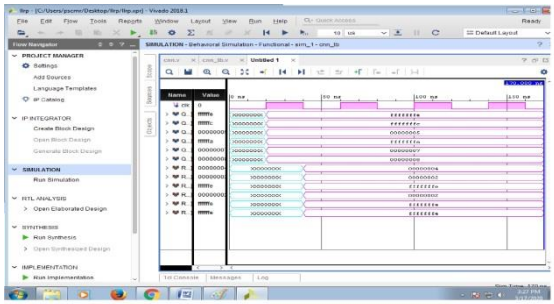
The above graph shows the input message bits that are transmitted to the encoder. The message bits are in the form of binary bits, 0 and 1. Here we considered 16 message bits.

Output of encoder



The above two figures shows the output of the encoder. The first 16 bits in the output are the message bits and the next 16 bits are parity bits

Check node output



Check node performs the row operation. In the above figure the output represents the row operation where the min sum operation is performed. Firstly it considers the two min bits without considering the sign and replaces the two min values with each other. The remaining values in the row are replaced by first min value. Finally the sign is checked and assigned based on the parity.

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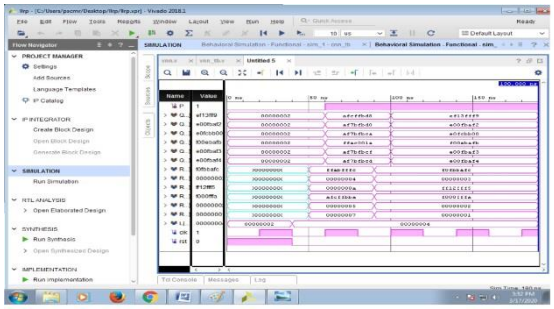
Variable node output



Variable node performs the column operation. It adds the entire columns and subtracts the added values with the received values from the channel.

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