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DESIGN OF FIR FILTER USING EFFICIENT ADDER AND MULTIPLIER FOR ECG SIGNAL PROCESSING APPLICATIONS

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Abstract

In this paper, we have to design an area and power efficient Finite impulse response (FIR) filter for Electrocardiogram (ECG) applications. Cardiovascular vascular is one erratic sickness on the planet. The traditional FIR filter expels undesirable noise in ECG signal yet this Filter consumes more power and possesses more regions, so we propose another power and region productive FIR filter. Area, power and delay are the key parameters for the design of FIR filter. The adder and multipliers plays a major role of designing of FIR Filter. The main aim of this paper is to design a FIR Filter using efficient carry select adder with booth multiplier. It is inferred from the presented results that the Power, area and delay of proposed FIR filter design using carry select adder with booth multiplier has been reduced notably compared to other Adders and Multipliers like Wallace tree multiplier, Array multiplier, Ripple carry adder, Carry skip adder and Carry look ahead adder. The design and Simulation of FIR filter is done by using modelsim13.1 and Quatras-2 power estimator tool with verilog HDL.

Keywords- **Carry select adder, booth multiplier, D flip-flop, Xilinx modelsim13.1 and Quatras-2, Matlab**.

I. INTRODUCTION

FIR filters are one of two essential kinds of Digital filter utilized in Digital Signal Processing (DSP) applications, the other sort being IIR. The ensuing filter approaches the perfect characteristic because the order of the filter will increase, so creating the filter and its implementation additional complicated. The design process starts with necessities and specifications the FIR filter. The method used in the design process of the filter depends upon the implementation and specifications. There are many advantages and disadvantages of the design methods. Statics demonstrates that over 70% guidelines in microchip and the majority of DSP calculations perform expansion and increase so, these tasks defeat the execution time. The interest of fast preparing has been expanding because of growing signal processing applications. To diminish noteworthy power utilization it is a great idea to decrease the quantity of activity accordingly diminishing unique power which is a major part of all out power utilization so the need of fast and low power multiplier has been use. Thus, it is very significant to elect the right method for FIR filter design. Usually these filters are designed with a multiplier, adders and a series of delays to create the output of the filter. Reconfigurable FIR filter auxiliary plans were accomplished for low power applications. Multiplication and Accumulation (MAC) unit estimates the duration of periodic impulses. Therefore, high performance of multiplication and accumulation architectures is required to improve the performance of digital FIR filter [1]. The filtering unit reduces noises such as baseline wander, power line interference and high-frequency noise using two stage finite-impulse response (FIR) filters [2].The implementation of an FIR filter requires three basic building blocks. They are Multiplication, Addition and delay components consume the most amount of area in a FIR filter design. As the multiplier is the slowest element in the system, it will affect the performance of the FIR filter [3]. The FIR filter consists of 'n' number of adders and 'n+1' number of multipliers. However, these filters are suffering from a large number of additions and multiplications [4].

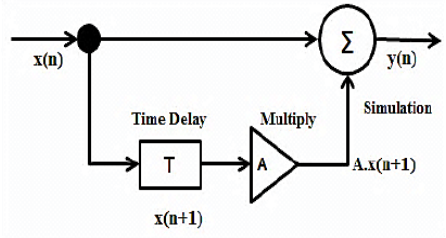

Figure 1. Block diagram of basic Digital filter

The rest of this paper is organized in five sections. Section 2 presents Literature survey. Section 3 describes the proposed work. The different types of Adders and Multipliers are presented in this section. Section 4

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presents the FIR filter structure. We present FIR filter implementation in section 5 shows the numerical results. Finally, conclusions are drawn in section 6.

II. LITERATURE SURVEY

In paper [1] author introduced a multiplier with SQRT CSLA is acquainted in this venture with increment the exhibition of MAC unit of advanced FIR filter. Repetitive rationale elements of both traditional multipliers and adders are recognized to expand the exhibition of MAC unit. Additionally Reduced multifaceted nature SQRT CSLA based Wallace tree Multiplier offers 6.4% decrease in silicon area and 36.58% decrease in deferral and 29.95% reduction of power utilization than the Ripple carry adder based filter structure.

In paper [2] author proposed FIR filter configuration is engaged utilizing quick FIR calculation with symmetric coefficients reworking and carry save addition. Static Timing Analysis (STA) is completed to discover the delay by including the individual gate delays and net postponements of every path. The improvement in SNR worth demonstrates that separating execution of FIR filter has upgraded because of limited progress band which thusly because of raise in the request for proposed FIR filter.

In paper[3] author projected modified booth multiplier and carry look ahead adder for FIR filter design. An exceptionally region proficient Finite Impulse Response filter dependent on altered Booth multiplier is structured and compared with traditional filter, in which decreases both area and delay.

In paper [4] author introduced FIR filter joined with the Wallace multiplier gives better filter execution in delay, area and power when contrasted with existing structures. Wallace multiplier successfully improves the proficiency of the FIR filter by making the performance faster, reducing the delay and area consumed.

In paper [5] author proposed a configuration utilizing RAG can give quicker speed and require less equipment assets than that for the Direct Structure-I plan. Proposed configuration can accomplish about 2% region delay and 43% less power utilizations in execution of a FIR low-pass filter than other research work

III. PROPOSED METHOD

Adders

A. ripple carry adder: The ripple carry adder is constructed by cascading full Adder blocks in series. The carry-out of one stage is fed directly to the carry- in of the next stage. For an n-bit ripple adder, it requires n full adders.

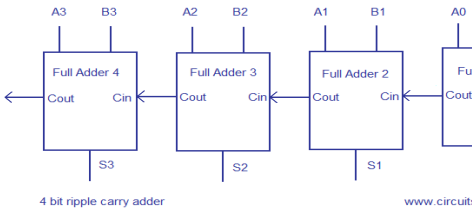

Figure2. 8 bit RCA adder

B. Carry skip adder:

A carry skip adder (otherwise called a carry bypass adder) is a adder usage that enhances the delay of a ripple carry adder with little exertion contrasted with different adders. The improvement of the most pessimistic scenario postponement is accomplished by utilizing a few carry skip adders to shape a square carry skip adder.

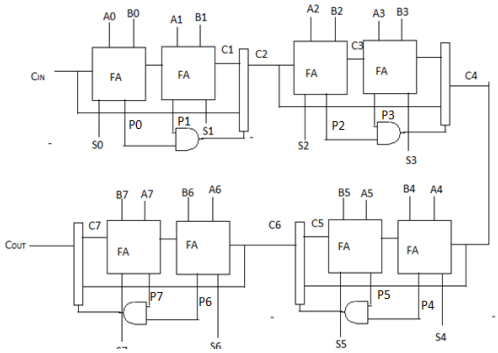

Figure3.8bit Carryskip adder.

C. Carry look ahead adder:

A carry look-ahead adder improves speed by decreasing the measure of time required to decide carry bits. It tends to be stood out from the more straightforward, yet normally slower, carry adder for which the carry bit is determined close by the total piece, and each piece must hold up until the past carry has been determined to start ascertaining its very own outcome and carry bits.

$Pi = Ai \oplus Bi$

$Gi = Ai*Bi.$

The output sum and carry can be defined as:

$S = Pi \oplus Ci.$

$Ci +1 = Gi + PiCi$

Gi is known as the carry Generate signal since a carry (Ci+1) is generated whenever Gi =1, regardless of the input carry (Ci).

Pi is known as the carry propagate signal since whenever Pi =1, the input carry is propagated to the output carry, i.e., Ci+1. = Ci

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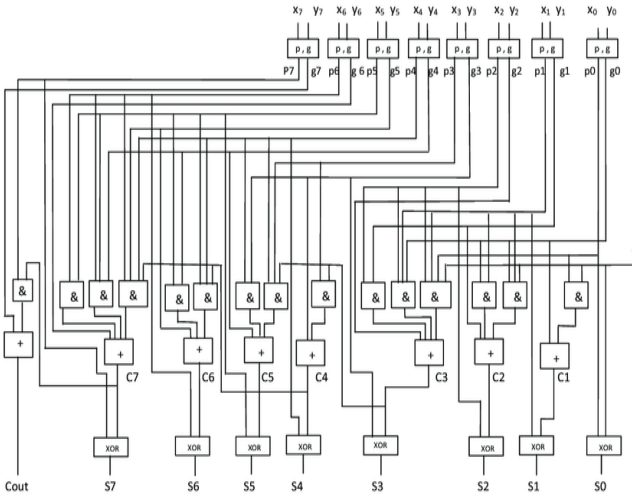

Figure4. 8bit CLA adder.

D. Carry select adder:

A carry select adder is an arithmetic combinational logic circuit which adds two N-bit binary numbers and outputs their N-bit binary sum and a 1-bit carry. **.**A 8-bit carry select adder, worked as a course from a 1-bit full-adder, a 3-bit carry select square, and a 4-bit carry select adder. A carry-select adder is an efficient parallel adder with O (n√n) delay (in its square root configuration) that adds two n-bit numbers.

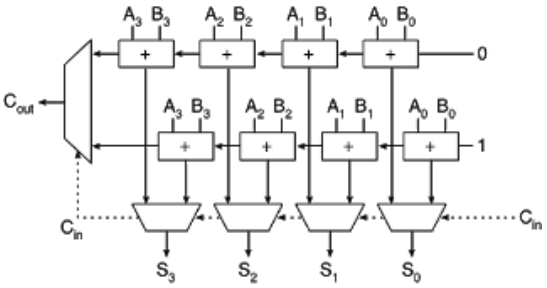

Figure5. 8bit CSA adder.

MULTIPLIERS:

A. Booth's algorithm for two complements multiplication:

1. Multiplier and multiplicand are placed in the Q and M register respectively.
2. Result for this will be stored in the AC and Q registers.
3. Initially, AC and Q_{-1} register will be 0.
4. Multiplication of a number is done in a cycle.
5. A 1-bit register Q_{-1} is placed right of the least significant bit Q_0 of the register Q.
6. In each of the cycle, Q_0 and Q_{-1} bits will be checked.
   i. If Q_0 and Q_{-1} are 11 or 00 then the bits of AC, Q and Q_{-1} are shifted to the right by 1 bit.
   ii. If the value is shown 01 then multiplicand is added to AC. After addition, AC, Q_0, Q_{-1} register are shifted to the right by 1 bit.
   iii. If the value is shown 10 then multiplicand is subtracted from AC. After subtraction AC, Q_0, Q_{-1} register is shifted to the right by 1 bit.

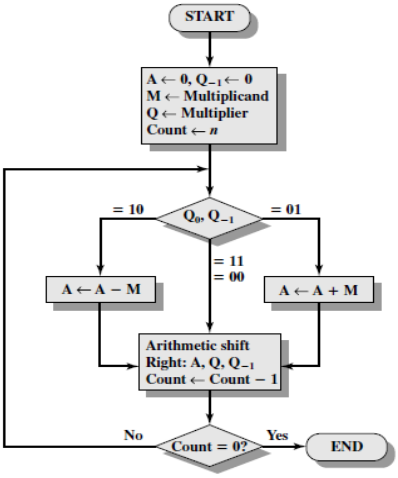

Figure6. 8*8 bit Booth multiplier.

B. Wallace tree multiplier:

A Wallace tree multiplier is an improved adaptation of tree based multiplier architecture. The multiplier naturally has the longest delay of any of the components used in our design. For this reason it was important to implement a multiplier design that would produce the smallest delay possible. The Wallace Tree Multiplier is more cost effective and has a shorter delay across the critical path because the number of adders needed on the critical path is reduced. Since the design uses fewer adders than other conventional designs, it is not only faster, but takes up less area and therefore cost less to manufacture. Another benefit to using less adders is that less transistors are needed, and therefore less power is consumed by the device. There is one disadvantage to a Wallace Tree multiplier however, and that is that it is difficult to manufacture efficiently due to its irregular layout.

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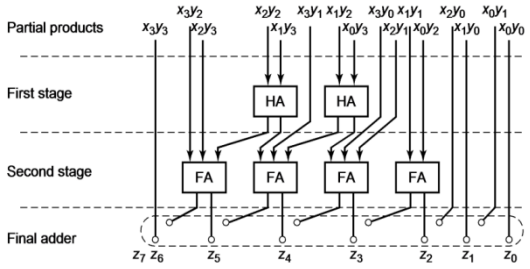

Figure7. 8*8 bit Wallace tree multiplier.

C.FIR Filter structure:

The following figure shows the basic FIR filter diagram with N length. The values of h(i) are the coefficients which are used for multiplication.

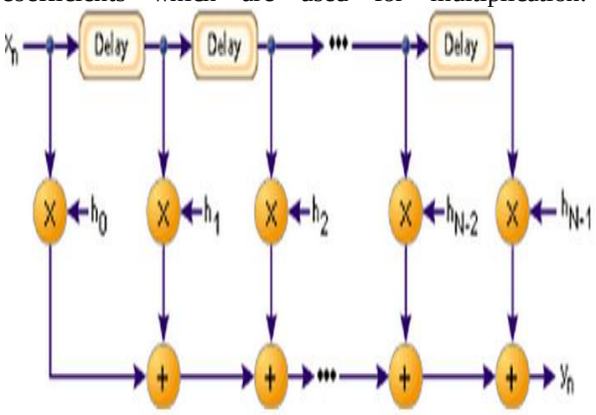

Figure9.structure of FIR filter.

For an N-tap FIR filter output function is defined as, y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2)+……h(N-1)x(n-N-1). In the proposed method multiplier replaced by booth multiplier and adder replaced by carry select adder.

IV. SOFTWARE AND HARDWARE USED

Xilinx ISE, MATLAB are the software used for Simulation and project is implemented using cyclone FPGA.

V. RESULTS AND DISCUSSIONS

Simulation was done by using the ModelSim 13.1 simulator. Parameters like area and delay can be analyzed by using Xilinx ISE 10.1 simulator. Power calculated by using Quartus2 power analyzer. The simulation results of different types of adders are shown below.

ADDERS

Simulation Results

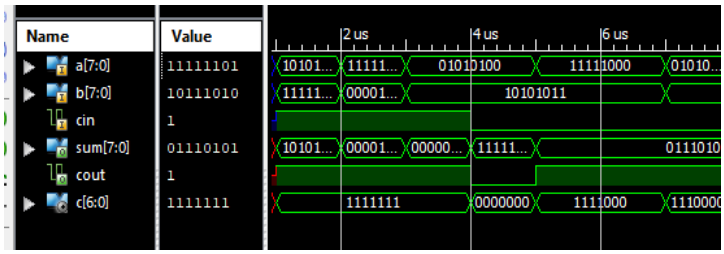

Figure 10.simulation Result of RCA Adder

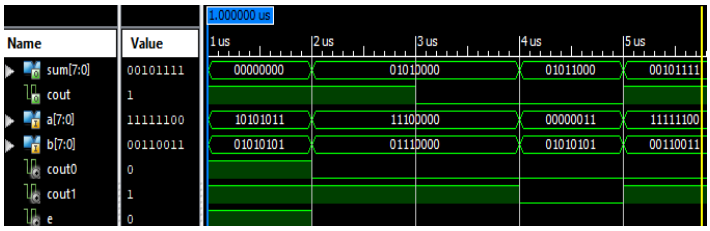

Figure 11.simulation Result of carry skip Adder

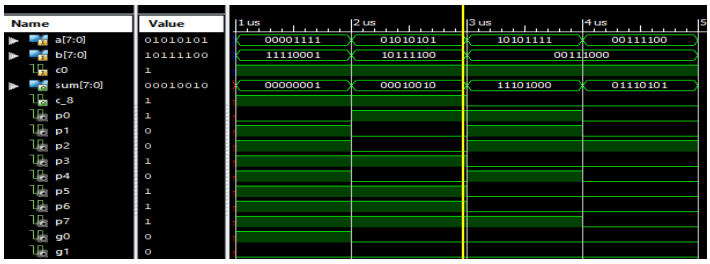

Figure 12.simulation Result of CLA adder

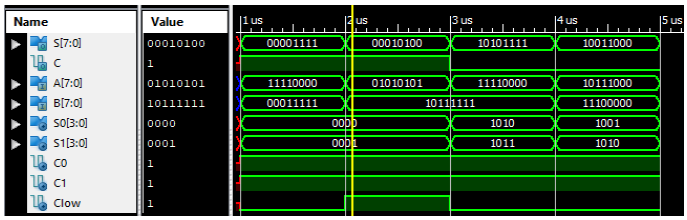

Figure 13. simulation Result of CSA Adder

After observation of simulation waveforms, synthesis is performed for calculation of delay and area and comparison of adder and multipliers are made in terms ofpower, area and delay and listed in the below table1 and table 2.Table1.Comparison of Adders

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Adder	No of slices	No of LUT	No of IOBS	Memory usage	Power consumption (mW)	Delay(ns)
RCA	12	16	25	4520260 (kb)	194.84mW	13.20ns
Carry skip	11	18	25	4520252 (kb)	196.09mW	12.057ns
CLA	12	16	26	4520256 (kb)	196.26mW	13.164ns
CSA	10	18	25	4520264 (kb)	196.02mW	10.061ns

MULTIPLIERS:

BOOTH MULTIPLIER

Multipliers	No of slices	No of LUT	No of IOBS	Memory usage	Power consumption (mW)	Delay (ns)
Wallace tree	88	156	32	4536476 (kb)	196.06mW	10.67 ns
Booth	28	43	35	4520244 (kb)	197.33mW	5.032 ns
Vedic	85	152	32	4536468(kb)	196.84mW	17.689ns
Array	44	74	16	4536472(kb)	195.05mW	11.435ns

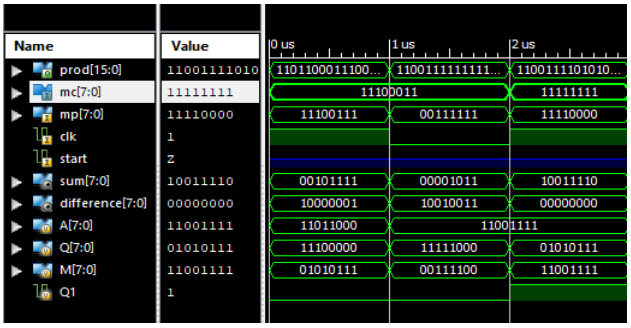

Figure14.simulation Result of Booth multiplier.

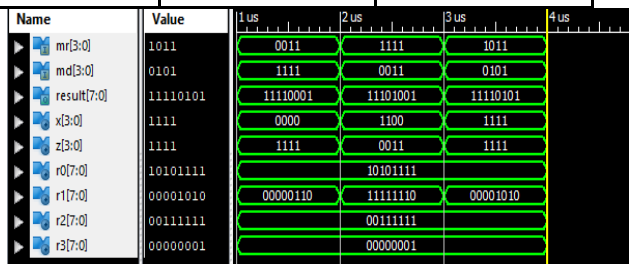

Figure 1 5.simulation Result of Wallace tree multiplier

Table2.comparsion of multipliers

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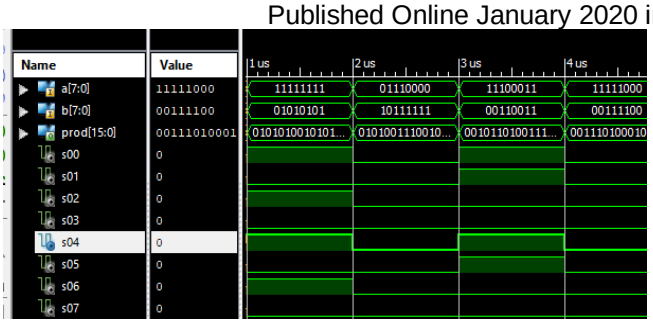

Figure 16.simulation Result of Array multiplier.

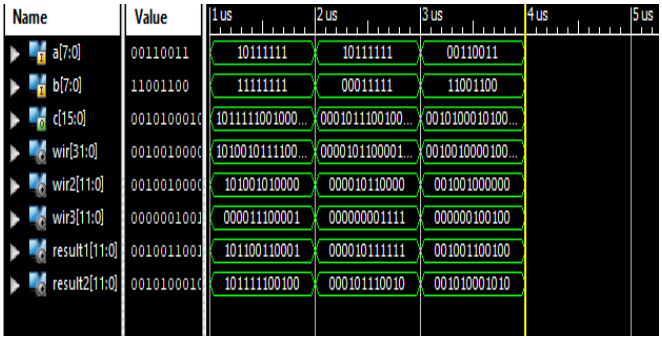

Figure 17.simulation result of Vedic multiplier.

From the above results Carry select adder and Booth Multiplier achieve efficient power area and delay. So we have to design a filter using CSA with Booth multiplier. The simulation results of FIR filter shown in below.

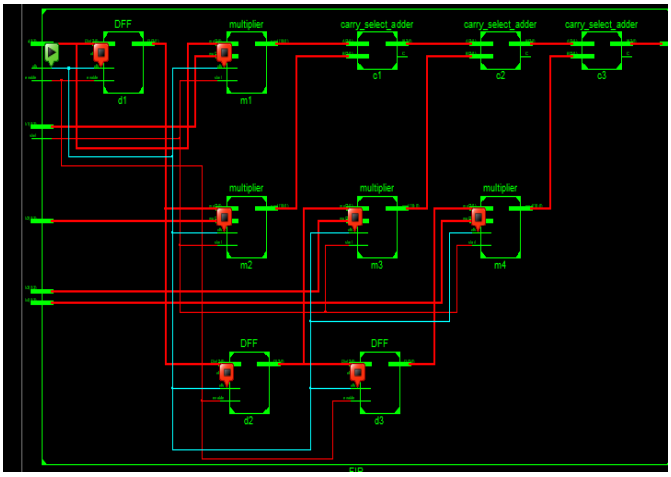

Figure18. Schematic RTL logic of FIR filter.

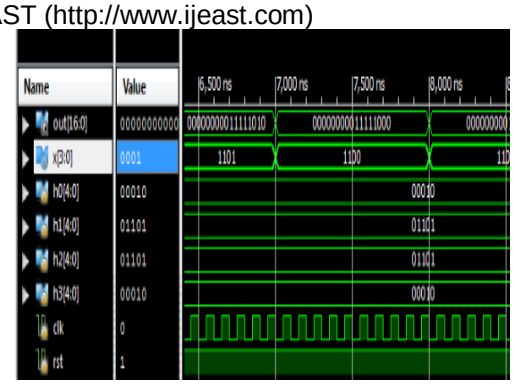

Figure 19.simulation result of 4tap FIR filter.

Next we compute the filter coefficients by using MATLAB FDA tool. There are four coefficients and three delay cells in Figure (9). Steps to compute filter coefficients:

- Defining filter specifications;
- Specifying a window function according to the filter specifications;
- Computing the filter order required for a given set of specifications;
- Computing the window function coefficients;
- Round off the values;

The formula is simple: given a FIR filter which has N taps, the delay is: (N – 1) / (2 * Fs), where Fs is the sampling frequency.

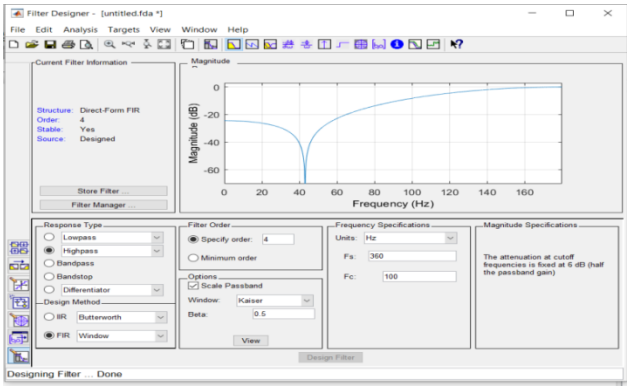

Figure 20.filter design using MATALAB FDA tool

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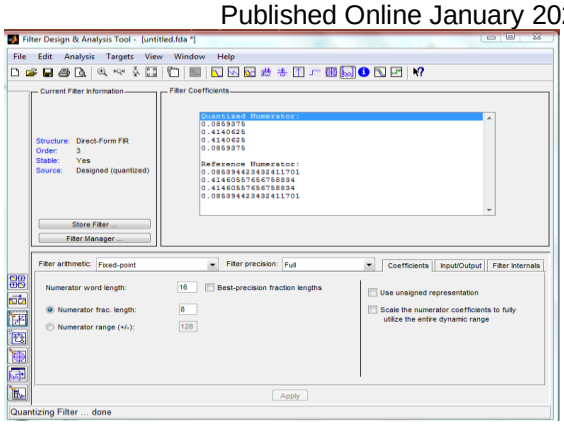

Figure21. Quantized filter coefficients.

VI. CONCLUSION

Structure upgrades are made regularly in the current gadgets for the best execution and proficiency. In this we have seen that FIR filter when incorporated with the Booth multiplier and carry select adder gives better filter performance in delay, area and power as compared to existing design. Booth multiplier adequately improves the proficiency of the FIR filter by making the performance faster; reduce the delay and area expended. This proposed design has efficient use in DSP applications, audio signal processing, medical signal applications etc. In future ECG signal can be analyzed by using adaptive filter.

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