International Journal of Engineering Applied Sciences and Technology, 2019
Vol. 4, Issue 6, ISSN No. 2455-2143, Pages 270-277
Published Online October 2019 in IJEAST (http://www.ijeast.com)

MODELLING AND OPTIMIZATION OF SUBTHRESHOLD LEAKAGE CURRENT IN LOW-POWER, SILICON-BASED, COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS) DEVICES

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Abstract*— The trend of process scaling for CMOS technology has made subthreshold leakage reduction a growing concern for submicron circuit designers. Power consumption has become a principle design consideration as device sizes decrease and many more devices fit on a single chip. Since switching power is proportional to the square of the supply voltage, v^2_{dd}, new processes are tailored for lower supply voltages. The decrease in V_{dd} slows down devices, which requires that the threshold voltage, V_{th}, must be lowered to maintain performance. This reduction of V_{th} produces the exponential increase of subthreshold leakage currents. This research demonstrates a process used to model and optimize subthreshold leakage current for a CMOS device during its standby mode (OFF-state). The process involves the use of MATHCAD to examine the OFF-state subthreshold leakage current, I_{sub} (OFF), based on variations in the threshold voltage, V_{th}, the effective transistor channel length, L, and the effective transistor channel width, W. The theoretical work entails simplifying the empirical relationship between the surface inversion potential, φ_s, the gate-source voltage, V_{gs}, and the subthreshold swing coefficient, n. This results in an expression relating the OFF-state subthreshold leakage current, I_{sub} (OFF), the threshold voltage, V_{th}, the effective transistor channel length, L, and the effective transistor channel width, W. Analyzing the resulting equation using MATHCAD confirms that the off-state subthreshold leakage current, I_{sub} (OFF) increases exponentially with a decrease in the threshold voltage, V_{th}, and linearly with a decrease in the effective transistor channel length, L. The results also show that the OFF-state subthreshold leakage current, I_{sub} (OFF), increases linearly with the effective transistor channel width, W. The optimization process resulted in the values of V_{th} = 140 mV, L = 28 nm and w= 7 nm which give the desired outcome of greatly reduced off-state subthreshold leakage current, I_{sub} (OFF) = 0.125 nA, for a single transistor.

Key words- MOS, CMOS, low power, threshold voltage, subthreshold leakage current, channel length, channel width, DIBL, load capacitance (C_L), supply voltage (V_{dd}), BSIM MOS.

I. INTRODUCTION

The increasing need of mobile communication represented by the mobile telephone has been showing remarkable growth. This market has been making tough demands for semiconductor Integrated Circuits (ICs) to consume less power, have higher integration, have multi-function capability and be faster. Problems of heat removal or cooling are worsening because the magnitude of power dissipated per unit area is growing with the increased integration of more components on a smaller surface area of a chip. This has led to rapid and innovative developments in low power designs during recent years.

To achieve a higher transistor density, lower power consumption and improved performance, MOS devices have been scaled for more than 30 years, Dutta (2016). As a result, transistor delay times decrease by more than 30% per technology generation, resulting in doubling of microprocessor performance every two years, Borkar (1999). Moore's law which states that: "The number of transistors on a chip doubles every 18 months" Moore (1965), has been held true for the last 40 years due to rapid progress and scaling (increased integration on a small surface area) of bulk Complementary Metal Oxide Semiconductor (CMOS) transistor technology. This motivates the need for CMOS scaling in the design of low power circuits in scaled technologies (that is, device feature sizes < 100 nm.) to meet low voltage and low

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power requirements. However, as a result of continued increased integration on a smaller surface area, the supply voltage, V_{dd}, has been scaled down to keep the power consumption under control. Hence, the transistor threshold voltage, V_{th}, has to be commensurately scaled to maintain a high drive current and achieve performance improvement. Threshold voltage scaling results in an exponential increase in the off-state leakage current known as sub-threshold leakage current, $I_{sub.}$ This becomes a crucial limiting factor for further down-scaling of the threshold voltage since it determines the power consumption of a chip in its idle state.

It has also been shown that the OFF-state subthreshold leakage current, I_{sub} (OFF), has increased by about five times per technological generation, due to the aggressive reduction of device size so that millions of devices can be integrated on a smaller chip area, for the last three generations. Consider an example of a cell phone chip containing one hundred million transistors; if I_{sub} (OFF) is a modest 100nA per transistor, the chip would consume so much standby current (10A) that the battery would be drained in minutes without receiving or transmitting any calls. A desktop Personal Computer chip may be able to tolerate this static power but not much more before facing expensive problems with cooling the chip and the system. This will adversely affect most low power devices (microelectronic systems) which usually operate primarily in bursts of activity amid significant periods of inactivity. Standby subthreshold leakage current reduction can reduce the power dissipation of such devices during these standby periods.

According to Tyagi (2007), effective channel length, L and gate oxide thickness, t_{ox} of 35nm and 1.2nm respectively have been demonstrated in the 65nm technology mode. This, however, cannot go beyond the limit, effective channel length L$\leq$ 10nm, which is subject to quantum mechanical tunneling effects which can initiate a damage leading to reliability concerns of the device. Consequently, there are increasing technology and design problems to be solved if Moore's law has to hold. These limitations include standby power leakage, Short Channel Effects (SCEs), parasitic capacitance issues and interconnect issues.

This paper presents a Silicon-based CMOS transistor model used to optimize the off-state subthreshold leakage current, I_{sub} by varying the threshold voltage, V_{th}, the channel length, L and the device width, W.

II. LEAKAGE CURRENT MECHANISMS IN SCALED CMOS DEVICES

Generally, in nanometer CMOS circuits, the main leakage current mechanisms are gate tunneling, reverse-biased junction band-to-band tunneling (BTBT) and sub-threshold leakage currents, as shown in Figure 1.

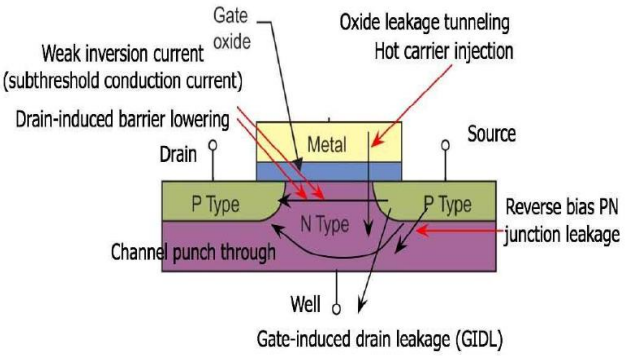

Figure 1: Major leakage mechanisms in MOS transistors, Butzen et al (2007).

Subthreshold Leakage Current

Subthreshold leakage current, I_{sub}, is defined as the drain-to-source leakage current when the transistor is OFF, Xu et al (2004), Deepaksubramanyan et al (2007), Vijayalakshmi (2017). It occurs between drain and source when the transistor is operating in the weak inversion region, that is, the gate voltage, V_g, is lower than the threshold voltage, V_{th}, that is, ($V_g < V_{th}$). In this region, supply voltage has been reduced so that the dynamic power consumption is controlled. The minority carrier concentration is almost zero, and the channel has no horizontal electric field, but a small longitudinal electric field appears due to the drain-to-source voltage. In this situation, the carriers move by diffusion between the source and the drain of the MOS transistor. Therefore, the subthreshold leakage current is dominantly due to the diffusion of carriers and it varies exponentially with both the gate-to-source and threshold voltages.

To maintain a high drive current capability, the threshold voltage, V_{th}, has to be reduced too. This, in turn, results in increase in the subthreshold leakage current. This is due to the fact that current does not drop abruptly to zero when $V_{gs} = V_{th}$. Furthermore, the drain current is not zero at zero gate voltage (and large drain voltages), indicating that the gate has lost control of shutting off the device, Yang (1988). Instead, the current decays off in an exponential fashion when $V_{gs} < V_{th}$. Thus, the output current cannot be turned OFF and the transistor can no longer function as a switch. However, this soft breakdown (exponential current decay) is not seen in long channel devices.

The threshold voltage, V_{th}, for a MOS device is the minimum voltage that will induce inversion layer which turns on the transistor. In order to take into account non-uniform substrate doping, the following standard threshold model by Gu et al (1996) was proposed,

$$V_{th} = V_{fb} + \phi_s + K_1\sqrt{\phi_s - V_{bs}} - K_2[\phi_s - V_{bs}] - \eta V_{ds} \quad (2.1)$$

where ϕ_s is the surface-inversion potential, K_1 and K_2 together model the body effect phenomenon, V_{ds} is the drain-to-source voltage, V_{bs} is the body bias voltage, η is the Drain Induced Barrier Lowering (DIBL) coefficient and V_{fb} is the flat-band voltage. In an idealized MOS

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structure, it is assumed that the energy-band diagram is flat when the gate voltage is zero. In practice, however, this condition is not realized because of unavoidable work function difference and charges in the oxide and surface states, Vijayalakshmi (2017). To achieve the flat-band condition for an NMOS, a negative gate voltage is applied to lower the electric field distribution until the charge is reduced to zero at the silicon surface. The gate voltage required to achieve the flat-band condition is known as the flat-band voltage, V_{fb}.

At values of the gate-source voltage, V_{gs} below the threshold voltage, V_{th}, the inversion electron concentration (n_s) is small but nonetheless can allow a small leakage current to flow between the source and the drain, I_{ds}. The differential equation for the surface-inversion potential, $\varphi_s$with respect to the gate-source voltage is given by Mookerjea (2009),

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{ox}}{C_{ox}+C_{dep}} \equiv \frac{1}{n} \qquad (2.2)$$

where the surface-inversion potential is, φ_s, C_{ox} is the gate oxide capacitance, C_{dep} is the capacitance of the depletion layer, n is the Subthreshold swing coefficient and V_{gs} is the gate-source voltage.

Considering the Berkeley Short-Channel IGFET Model for MOS transistors (BSIM MOS), Sheu (1987), Gu et al (1996), Manisha (2011), Singh et al (2013), Vijayalakshmi (2017), the subthreshold leakage current for a MOSFET device is expressed by,

$$I_{sub} = I_o . e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \qquad (2.3)$$

where V_{th} is the threshold voltage, V_{ds} and V_{gs} are drain-to-source and gate-to-source voltages, respectively and n is the subthreshold swing coefficient, for a long channel uniformly doped device given by,

$$n = 1 + \frac{C_b}{C_{ox}} \qquad (2.4)$$

where the parameters C_b and C_{ox} are the bulk (substrate) and the gate oxide capacitances, respectively. These are expressed by equations (2.5) and (2.6) respectively.

$$C_b = \frac{\varepsilon_{si}}{\omega_d} \qquad (2.5)$$

and,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (2.6)$$

where ε_{ox} and ε_{si} denote the dielectric constants of the oxide and silicon respectively, ω_d is the depletion width under the channel, and t_{ox} is the gate oxide thickness.
The practical definition of V_{th} in experimental studies is the gate-source voltage V_{gs} at which the drain to source current, I_{ds}, in nano-Amperes (nA) is given by,

$$I_{ds}(nA) = 100 \times \frac{W}{L} \times e^{\frac{q(V_{gs}-V_{th})}{nkT}} \qquad (2.7)$$

The 100 value in equation (2.7) is the value of the current at threshold I_o, in nA, and it is derived from,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L} \qquad (2.8)$$

The $e^{1.8}$ term was found empirically, Sheu (1987). C_{ox} is the gate oxide capacitance and μ_o is the carrier mobility. The parameter V_T is known as the thermal voltage and is expressed as,

$$V_T = \frac{kT}{q} \qquad (2.9)$$

where k is the Boltzmann's constant and T is the absolute temperature.

The carrier mobility μ_o is the proportionality constant between applied electric field (in V/cm) and the resulting velocity of the carriers (in cm/sec). The intrinsic values (for pure silicon) of the mobility for electrons and holes at room temperature (T= 300K) are, μ_n = 1350cm^2/V·s (for electrons) and μ_p = 480cm^2/V·s (for holes). The fact that holes are more sluggish than electrons has some influence on relative sizes of nMOS and pMOS transistors. The gate-oxide-channel structure forms a capacitor. The gate-oxide capacitance per unit area can be calculated from the equation (2.6), where, ε_{ox}= 0.351pF/cm is the permittivity (a dielectric constant) of SiO_2. Note that this capacitance is inversely proportional to the thickness of the silicon-dioxide layer. The oxide thickness and the resulting gate capacitance per unit area are parameters specified by the technological process of fabrication of CMOS transistors.

For example, consider a typical 65 nm technology nMOS transistor at Vgs= 1.0 V, where the gate oxide thickness, t_{ox}, used was 194 nm and V_T^2 at room temperature was 6.76 × 10^{-6} V^2, Weste et al (2016), then,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.51\times10^{-13}}{1.94\times10^{-7}} = 1.81 \times 10^{-6}\text{F/cm}^2 \qquad (2.10)$$

and,

$$\mu_o C_{ox} V_T^2 e^{1.8} = 1350 \times 1.81\times 10^{-6} \times 6.76 \times 10^{-6} \times 6.0497$$
$$= 9.99\times10^{-8}\text{ A}$$
$$\approx 100\text{ nA} \qquad (2.11)$$

In practice, this value (2.11) is usually set by CMOS manufacturing Companies, during fabrication, to either 100 nA or 200 nA. The choice of this value by a Company to be 100 nA or 200 nA depends on the carrier mobility, μ_o, the gate oxide capacitance, C_{ox}, the device geometry and the thermal voltage, V_T the Company has adopted for fabrication of the transistor. For lower subthreshold leakage current, I_{sub}, a lower value is desirable, hence the choice of 100 nA in equation (2.7).

The empirical value of the channel length L, is 10 nm; which is the minimum value of L before quantum

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mechanical tunneling effects set in, while that of the channel width W= 7 nm; which approximates the current design minimum device width, and V_{gs} =0. The current through the device is measured for values of V_{th}= 0 to 300 mV. The 300 mV value approximates the upper edge of the subthreshold region for the CMOS devices, Deepaksubramanyan et al (2007), Weste et al (2016).

On a graph of I_{ds} versus Vgs, with logarithmic (base 10) axis for I_{ds}, the subthreshold slope is found as the straight-line approximation of the subthreshold current, normally expressed in units of decades/mV. The Subthreshold swing is the inverse of this slope and is expressed in units of mV/decade. Ideally, it is assumed that the current will drop as fast as possible once $V_{gs}<V_{th}$. However, in real transistors, current does not abruptly cut off below threshold voltage, but rather drops off exponentially as shown in Figure 2,

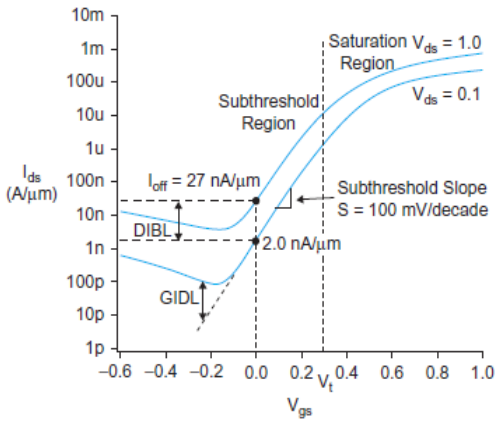

Figure 2: I-V characteristics of a 65 nm nMOS transistor at 70°C on a log scale, Weste et al (2016).

When the gate voltage, V_{gs} is high, the transistor is strongly ON. When the gate voltage falls below the threshold voltage, that is $V_{gs}<V_{th}$, the exponential decline in current appears as a straight line on a semi-logarithmic plot of I_{ds} against V_{gs}. The inverse of the slope of this line is known as the subthreshold swing, S, in millivolts per decade (mV/ decade), Manisha (2011), Singh et al (2013), Roy et al (2007), Weste et al (2016), given by,

$$S = \left[\frac{d(log_{10} I_{ds})}{dV_{gs}}\right]^{-1} \quad (2.12)$$

This is alternatively defined by,

$$S = n\left[\frac{kT}{q}\right] \ln 10 \quad (2.13)$$

Since $\ln 10 = 2.3$,

$$S = 2.3n\frac{kT}{q} \quad (2.14)$$

Substituting equation (2.4) into equation (2.14) for n, the subthreshold swing, S is found to be,

$$S = 2.3\frac{kT}{q}\left[1 + \frac{C_b}{C_{ox}}\right] \quad (2.15)$$

The subthreshold swing describes the exponential behavior of the current as a function of voltage. It also indicates how effectively the transistor can be turned off, that is, the rate of decrease of I_{OFF}, when V_{gs} is decreased below V_{th}. Practically, S can range from 70 to 120 mV/decade for a bulk CMOS process, while the subthreshold swing coefficient, n ranges between 1 and 2, Deepaksubramanyan et al (2007), Weste et al (2016).
As device dimensions and the supply voltage are scaled down to enhance performance, power efficiency and reliability, subthreshold leakage current may limit the scalability of the supply voltage.

III. METHODOLOGY

In this section, the equation used in MATHCAD to examine the effect of varying the threshold voltage, V_{th}, the transistor's channel width, W and its effective length, L on the off-state subthreshold leakage current, I_{sub} (OFF) is derived.

Derivation of the simulation equation

In a practical CMOS transistor, the drain-source current, I_{ds} is exponentially proportional to the surface inversion potential, φ_s, that is,

$$I_{ds} \propto e^{\frac{q\varphi_s}{kT}} \quad (3.1)$$

Now, the derivative of the surface inversion potential, φ_s, against the gate to source voltage, V_{gs} is given by,

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{ox}}{C_{ox}+C_{dep}} \equiv \frac{1}{n} \quad (2.2)$$

Rewriting equation (2.2) implies that,

$$n = 1 + \frac{C_{dep}}{C_{ox}} \quad (2.4)$$

Integrating equation (2.2), that is,

$$\int d\varphi_s = \frac{1}{n}\int dV_{gs} \quad (3.2)$$

or,

$$\varphi_s = constant + \frac{V_{gs}}{n} \quad (3.3)$$

where the constant parameter in equation (3.3), is,

$$constant = \frac{-V_{th}}{n} \quad (3.4)$$

then by using equations (3.3) and (3.4) in the index of the exponential of proportionality (3.1), results in,

$$I_{ds} \propto e^{q\left(\frac{-V_{th}}{n}+\frac{V_{gs}}{n}\right)/kT} \quad (3.5)$$

and,

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$$I_{ds} = I_o\, e^{q\left(\frac{-V_{th}}{n}+\frac{V_{gs}}{n}\right)/kT} \qquad (3.6)$$

where,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{\frac{qV_{gs}}{nkT}}}{L}\left(1-e^{\frac{-V_{ds}}{V_T}}\right) \qquad (3.7)$$

Using equations (2.9) and (2.13), equation (3.7) simplifies to,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{\frac{V_{gs}\ln 10}{S}}}{L}\left(1-e^{\frac{-V_{ds}}{V_T}}\right) \qquad (3.8)$$

Now, at threshold,

$$I_o = \frac{W\mu_o C_{ox} V_T^2 e^{1.8}}{L} \qquad (2.8)$$

When evaluated gives (refer to results 2.10 and 2.11),

$$I_o = \frac{100\,W}{L} \qquad (3.9)$$

Now, from equation (2.8), (2.9), result (2.11) and equation (3.6),

$$I_{ds} = I_o\, e^{\left(\frac{(V_{gs}-V_{th})\ln 10}{S}\right)} \qquad (3.10)$$

When the CMOS device is in standby mode the leakage current, I_{ds}, is also referred to as the subthreshold leakage current, I_{sub} (also denoted as I_{OFF}). In this OFF-state, V_{gs} =0, thus equation (3.10) is rewritten as,

$$I_{sub} = I_o\, e^{\left(\frac{-V_{th}\ln 10}{S}\right)} \qquad (3.11)$$

This simplifies to,

$$I_{sub} = I_o \times 10^{\frac{-V_{th}}{S}} \qquad (3.12)$$

Thus by using equations (3.9) and (3.12),

$$I_{sub} = 100 \times \frac{W}{L} \times 10^{\frac{(-V_{th})}{S}} \qquad (3.13)$$

Thus, the characteristics of subthreshold leakage current in the OFF state, I_{sub} (in nA) when the threshold voltage, V_{th} and device dimensions (channel length, L and width, W) are varied, can be determined by the model equation (3.13).

IV. RESULTS AND DISCUSSIONS

Effect of threshold voltage, V_{th} on the OFF-state subthreshold leakage current, I_{sub}

The subthreshold swing, S in equation (3.13) is varied through S= 60, 90 and 120 mV/decade while the values of W and L are set at 7 nm and 10 nm respectively.

Substituting the values of S, W and L respectively, into the model equation (3.13), three equations (4.1), (4.2) and (4.3) are obtained.

$$I_{sub1}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{60}} \qquad (4.1)$$

$$I_{sub2}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{90}} \qquad (4.2)$$

$$I_{sub3}(OFF)(A) = 100 \times 7.0 \times 10^{-10} \times 10^{\frac{-V_{th}}{120}} \qquad (4.3)$$

Figure 3 shows plots of the data obtained from equations (4.1), (4.2) and (4.3) where the leakage current, I_{sub} is plotted against the threshold voltage, V_{th} for different values of the subthreshold slope factor, S.

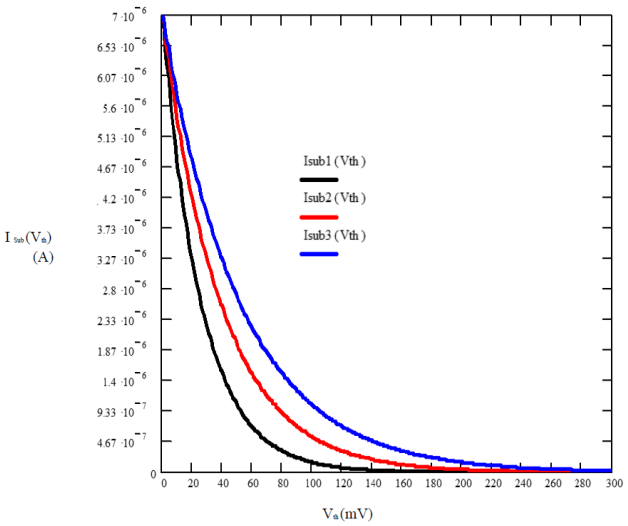

Fig 3: Variation of I_{sub} with V_{th}.

These graphs show that the leakage current, I_{sub} decreases exponentially with increase in the threshold voltage, V_{th}. The graphs also show that for a scaled CMOS device, whose channel length, L= 10 nm, the channel width, W= 7 nm, V_{gs} =0 (OFF-state) and the subthreshold swing, S= 60 mV/decade, the threshold voltage, V_{th} that results in zero OFF-state subthreshold leakage current, $I_{sub}\,(OFF)$, is about 140 mV. Increasing the subthreshold swing, S to 90 mV/decade increases the threshold voltage, V_{th} for zero OFF-state subthreshold leakage current, $I_{sub}\,(OFF)$ to about 180 mV. Further increment of the subthreshold swing, S to 120 mV/decade proportionally increases the threshold voltage, V_{th} for zero OFF-state subthreshold leakage current, $I_{sub}\,(OFF)$ to about 240 mV.

Thus, for minimum leakage current, low values of the threshold voltage, V_{th} = 140 mV and subthreshold swing, S of 60 mV/decade, are desirable.

Effect of Channel width, W on the OFF-state subthreshold leakage current, I_{sub}

The current through the device is measured for values of W ranging from 7 nm to 32 nm while the subthreshold swing, S

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in equation (3.13) is varied through S= 60, 90 and 120 mV/decade. The values of V_{th} and L are set at 300 mV and 10 nm respectively.

Substituting these values of S, L and V_{th} in the model equation (3.13) results in equations (4.4), (4.5) and (4.6).

$$I_{sub1}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{60}} \quad (4.4)$$

$$I_{sub2}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{90}} \quad (4.5)$$

$$I_{sub3}(OFF)(A) = 100 \times \frac{W}{10} \times 10^{-9} \times 10^{\frac{-300}{120}} \quad (4.6)$$

Figure 4 shows plots of the data obtained from equations (4.4), (4.5) and (4.6) where the off-state subthreshold leakage current, I_{sub} is plotted against the device's channel width, W, for different values of the subthreshold slope factor, S.

From the graphs it is seen that the OFF-state subthreshold leakage current, I_{sub} , increases almost linearly with increase in the channel width, W, on first approximation. The graphs also show that when the subthreshold slope factor, S= 60 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increases almost linearly from an approximate minimum of 1.0 pA to a maximum value of about 50 pA. When the subthreshold slope factor, S= 90 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increases almost linearly from approximately 0.05 nA to a maximum value of about 0.1 nA.

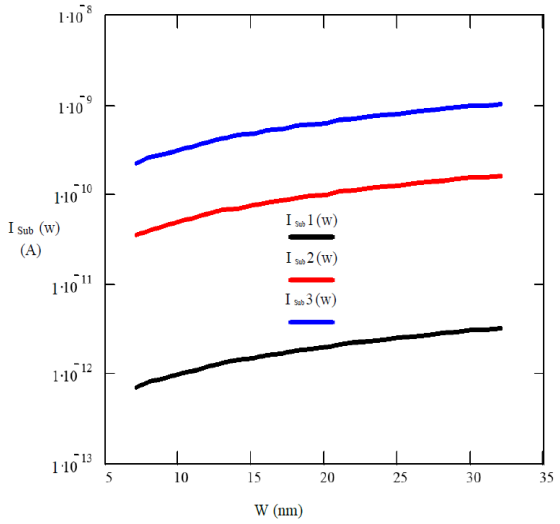

Fig 4: Variation of I_{sub} with W

When the subthreshold slope factor, S was further increased to 120 mV/decade, the OFF-state subthreshold leakage current, I_{sub} increased almost linearly from approximately 0.5 nA to a maximum value of about 1.0 nA. Thus, for minimum leakage current, a low value of the subthreshold slope factor, S of 60 mV/decade, is desirable.

It can also be seen that for a Silicon-based CMOS device, of minimum length, L= 10 nm and V_{gs} =0 (OFF-state), whose threshold voltage, V_{th} has been scaled to 300 mV and with a subthreshold swing, S of 60 mV/decade, the channel width, W, should be about 7 nm for minimal I_{sub}. ($I_{sub} \approx$ 0.8 pA).

Effect of Channel length, L on the OFF-state subthreshold leakage current, I_{sub}

For the simulation process, the subthreshold swing, S is varied through three different values of S= 60, 90 and 120 mV/decade. The current through the device is measured over this range of S, for the empirical value of V_{th} of 300 mV and L ranging from 10 nm to 28 nm, respectively.

Substituting these values of S, W and V_{th} in the model equation (3.13) results in equations (4.7), (4.8) and (4.9).

$$I_{sub1}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{60}} \quad (4.7)$$

$$I_{sub2}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{90}} \quad (4.8)$$

$$I_{sub3}(OFF)(A) = 100 \times \frac{7}{L} \times 10^{-9} \times 10^{\frac{-300}{120}} \quad (4.9)$$

Figure 5 shows plots of the data obtained from equations (4.7), (4.8) and (4.9) where the OFF-state subthreshold leakage current, I_{sub} is plotted against the channel length, L for values of the subthreshold slope factor S= 60, 90 and 120 mV/ decade.

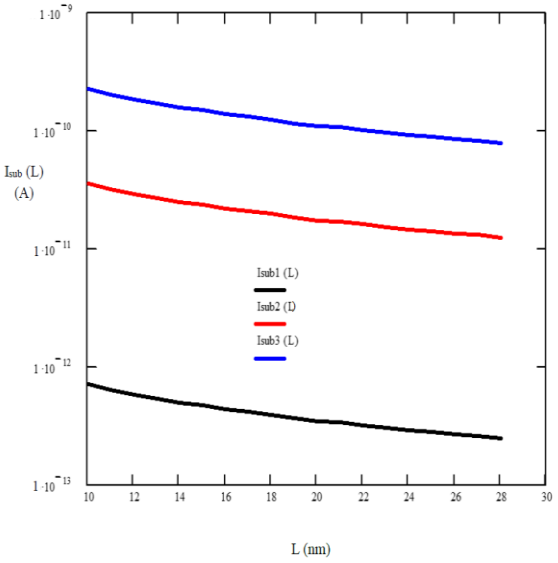

Fig. 5: Variation of I_{sub} with L.

The graphs show that the OFF-state subthreshold leakage current, I_{sub} (OFF) decreases almost linearly on first approximation with increase in the effective channel length, L of a Silicon-based CMOS transistor. The graphs also show that when the subthreshold swing, S= 60 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreases almost linearly from an approximate maximum of 8.0 pA to a minimum value of about 5.0 pA. When the subthreshold swing, S= 90 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreases almost linearly from an approximate maximum value of 50 pA to a minimum value of about 10 pA. When the subthreshold swing, S was further increased to 120 mV/decade, the OFF-state subthreshold leakage current, I_{sub} decreased almost linearly from an approximate maximum value of 0.5 nA to an approximate minimum value of about 0.1 nA. It can also be seen that, the OFF-state subthreshold

International Journal of Engineering Applied Sciences and Technology, 2019
Vol. 4, Issue 6, ISSN No. 2455-2143, Pages 270-277
Published Online October 2019 in IJEAST (http://www.ijeast.com)

leakage current, I_{sub} was much higher when S was raised to 90 and 120 mV/decade than when S was set at 60 mV/decade, shown by the wider gap between the former ranges of S and the latter.

Summary

The optimization of the OFF-state subthreshold leakage current in section IV indicates that the values of L and W should be 28 nm and 7nm, respectively, while the threshold voltage should be scaled to V_{th}= 140 mV. The value of the subthreshold swing should be set at 60 mV/decade for reduced OFF-state subthreshold leakage current, I_{sub}.

Given that the subthreshold slope factor S is 60 mV/decade and the values of the transistor effective channel length, L is 28 nm, its channel width, W is 7 nm and the threshold voltage, V_{th} is 140 mV, then by equation (3.13), the value of the OFF-state subthreshold leakage current, I_{sub} (OFF) for a single CMOS device will be,

$$I_{sub}(OFF)(A) = 100 \times \frac{7}{28} \times 10^{-9} \times 10^{\frac{-140}{60}} \quad (4.10)$$

$$I_{sub}(OFF)(A) = 1.25 \times 10^{-10} A$$

$$I_{sub}(OFF)(nA) = 0.125\ nA \quad (4.11)$$

The result obtained from equation (4.11) is then compared with those obtained for a typical 65 nm technology Silicon-based CMOS transistor, for the dimensions; L= 65 nm and W= 90 nm in order to illustrate its efficacy. In the comparison data, the Drain Induced Barrier Lowering coefficient, Ƞ, was set at Ƞ =0.1 and the subthreshold swing, S, at S =100 mV per decade, Weste et al (2016), Lale et al (2017). When the threshold voltage, V_{th}= 300 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 100 nA, whereas when the threshold voltage, V_{th}= 400 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 10 nA, and for the threshold voltage, V_{th}= 500 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 1.0 nA.

In another comparison data, Peng (2016), the transistor parameters used were: Transistor effective length, L= 20.7 nm, Channel Width, W= 6.5 nm, the subthreshold swing, S, was set at S =83 mV per decade. When the threshold voltage, V_{th}= 170 mV, the OFF-state subthreshold leakage current, I_{sub} (OFF) = 3.8 nA.

The result obtained from equation (4.10) indicates a comparatively reduced OFF-state leakage current. This reduction in leakage current will result in the CMOS device's high performance speed and lower power consumption.

V. CONCLUSION

In this research, modelling and optimization of the OFF-state Subthreshold leakage current, I_{sub}(OFF), in a Silicon-based CMOS transistor was done based on the variations in the threshold voltage, V_{th} and the device dimensions, that is, the effective channel length, L and the effective channel width, W. A model equation (3.13), giving the relationship of these parameters, was derived and analysed using MATHCAD.

From the analysis of the model equation, it was observed that, for a Silicon-based CMOS transistor,

i) The OFF-state subthreshold leakage current, I_{sub} decreases exponentially with increase in the threshold voltage, V_{th}.

ii) The OFF-state subthreshold leakage current, I_{sub}, increases almost linearly with increase in the channel width, W, on first approximation.

iii) The OFF-state subthreshold leakage current, I_{sub} (OFF) decreases almost linearly, on first approximation, with increase in the effective transistor's channel length, L.

iv) To obtain a relatively low OFF-state subthreshold leakage current, I_{sub} (OFF) for a single CMOS transistor, the values of the parameters in the model equation (3.13) should be set at; the threshold voltage, V_{th} = 140 mV, the effective transistor channel length, L= 28 nm and the effective transistor width, W= 7nm.

It can also be deduced that, for given W and L, three options can be adopted as ways of minimizing I_{sub}. These include;

i. Choosing a large V_{th}. This is, however, not desirable since a large V_{th} reduces the ON-current (I_{on}) and therefore increases the gate delays.

ii. Reducing the subthreshold swing, S by using a lower value of n. This can be achieved by increasing the gate oxide capacitance, C_{ox}, that is, by using a thinner gate oxide material, and decreasing the capacitance of the depletion layer, C_{dep}, the latter being achieved by increasing W.

iii. Additionally, the transistor is operated at a lower temperature. Low operational temperature results in a low subthreshold slope factor, S as shown by equation (2.13). This last approach is valid in principle but rarely used because cooling adds considerable costs.

As the channel width, W increases, the carrier density of the device also increases. This results in more carriers tunneling across the source-drain channel below the gate, hence increasing I_{sub}. Increase in the subthreshold slope factor, S also causes an increase in the OFF-state subthreshold leakage current, I_{sub}. The subthreshold slope factor, S indicates how much the gate voltage, V_{gs} must drop to decrease the leakage current by an order of magnitude.

Thus, for minimum leakage current, a high value of L= 28 nm and a low value of the subthreshold swing, S of 60 mV/decade, are desirable.

The graphs also show that for a Silicon-based CMOS device, of channel width, W= 7 nm and V_{gs} =0 (off-state), whose threshold voltage, V_{th} has been scaled to 300 mV and with a subthreshold swing, S of 60 mV/decade, the effective channel length should be about, L= 28 nm for minimal I_{sub}. ($I_{sub} \approx 0.5\ pA$).

The optimized values obtained in this research can be adopted by manufacturers of Silicon-based VLSI chips in order to take advantage of scaling of CMOS devices while still keeping the OFF-state subthreshold leakage current, I_{sub}(OFF) at a manageable minimum.

Future works also need to explore the possibility of varying the CMOS transistor's doping concentration so as to

determine the relationship between the concentration and the OFF-state subthreshold leakage current, I_{sub}.

VI. REFERENCES

[1]. Borkar, S. (1999). Design Challenges of Technology Scaling. *Proceedings of the IEEE Custom Integrated Circuits Conference*, New York, Vol. 10 (1) (pp. 23).

[2]. Butzen, P.F. and Ribas, R.P. (2007). Leakage current in sub micrometer CMOS gates. *Proceedings of the South symposium on microelectronics*, Vol. 22, Porto Alegre. (pp. 47-50).

[3]. Deepaksubramanyan, B.S. and Nunez, A. (2007). Analysis of Subthreshold Leakage Reduction in CMOS Digital Circuits. *Proceedings of the 13th NASA VLSI Symposium*, Post Falls, Idaho, USA. (pp. 1-7).

[4]. Dutta, S. (2016). Recent advances in High Performance CMOS transistors: From Planar to Non Planar. *The Electrochemical Society Interface*, Pennsylvania State University, Vol. 10, (2) (pp. 41).

[5]. Gu, R.X. and Elmasry, M.I. (1996). Power Dissipation analysis and optimization of Deep submicron CMOS digital circuits. *IEEE Journal of solid state circuits*, Vol. 31 (5), New York, (pp. 707-713).

[6]. Lale, A., Grappin, A., Mazenq, L., Bourrier, D., Lecestre, A., Launay, J. and Temple-Boyer, P. (2017). Development of All-round SiO_2/ Al_2O_3 Gate, Suspended Silicon Nanowire Chemical Field Effect Transistors Si-nw-ChemFET. *Proceedings of the Eurosensors 2017 conference*, Vol. 1 (1), Paris. (pp. 419).

[7]. Manisha, P. (2011). Analysis and Simulation of Subthreshold Leakage Current reduction in IP3 SRAM Bit-cell at 45nm CMOS technology for multimedia applications. *International Journal of Computer Theory and Engineering*, Vol. 3 (6), New York, (pp. 738).

[8]. Mookerjea, S. (2009). *IEEE International Electron Devices Meeting (IEDM), Digest of technical papers,* New York, (pp. 949).

[9]. Moore, G.E. (1965). Cramming more components onto integrated circuits. *Electronics.* New York: McGraw Hill Inc. (pp. 144).

[10]. Peng, Z. (2016). Advanced MOSFET Structures and Processes for Sub- 7nm CMOS Technologies. Doctor of Philosophy Thesis, University of California at Berkeley, 2016, (pp. 9-11).

[11]. Roy, K. and Prasad, S.C. (2007). Leakage current mechanisms and leakage reduction techniques in Deep sub-micrometer CMOS circuits. *Proceedings of IEEE*. Vol. 91 (2), New York, (pp. 305-327).

[12]. Sheu, B.J. (1987). BSIM: Berkeley Short-Channel IGFET Model for MOS transistors**.** *IEEE journal of Solid State Circuits,* SC-22, (No. 4), New York, (pp. 558-566).

[13]. Singh, S.K., Kaushik, B.K., Chauhan, D.S. and Kumar, S. (2013). Reduction of Subthreshold Leakage in MOS transistors. *World Applied Science Journal*, Vol. 3, Idosi Publications, (pp. 447).

[14]. Tyagi, S. (2007). Moore's law: A CMOS scaling perspective. *Proceedings of the 14th International symposium on the Physical and Failure Analysis of the Integrated Circuits*, New York, Vol. 5 (6), (pp. 10-15).

[15]. Vijayalakshmi, D. (2017). Estimation of New Accurate Subthreshold and Gate Leakage Current. *International Journal of Exploring Emerging Trends in Engineering (IJEETE)*, New York, Vol. 1 (1), (pp. 8-21).

[16]. Weste, N.H. and Harris, D. M. (2016). CMOS VLSI Design: A Circuits and Systems Perspective. 4th Edition. Boston: Addison-Wesley Inc. (pp. 61-87).

[17]. Xu, Y.J., Luo, Z.Y., Li, X.W., Li, L.J. and Hong, X.L. (2004). Leakage Current Estimation of CMOS Circuits With Stack Effect. *12th IEEE Asian Test Symposium*, Xian, China, Vol. 19 (5), (pp. 708- 717).

[18]. Yang, E. (1988). Microelectronic Devices. New York: McGraw Hill Inc. (pp. 209-296).